

FM9 XXXX Intel Discrete GFX

VER : 1A

PWA:

PWB:

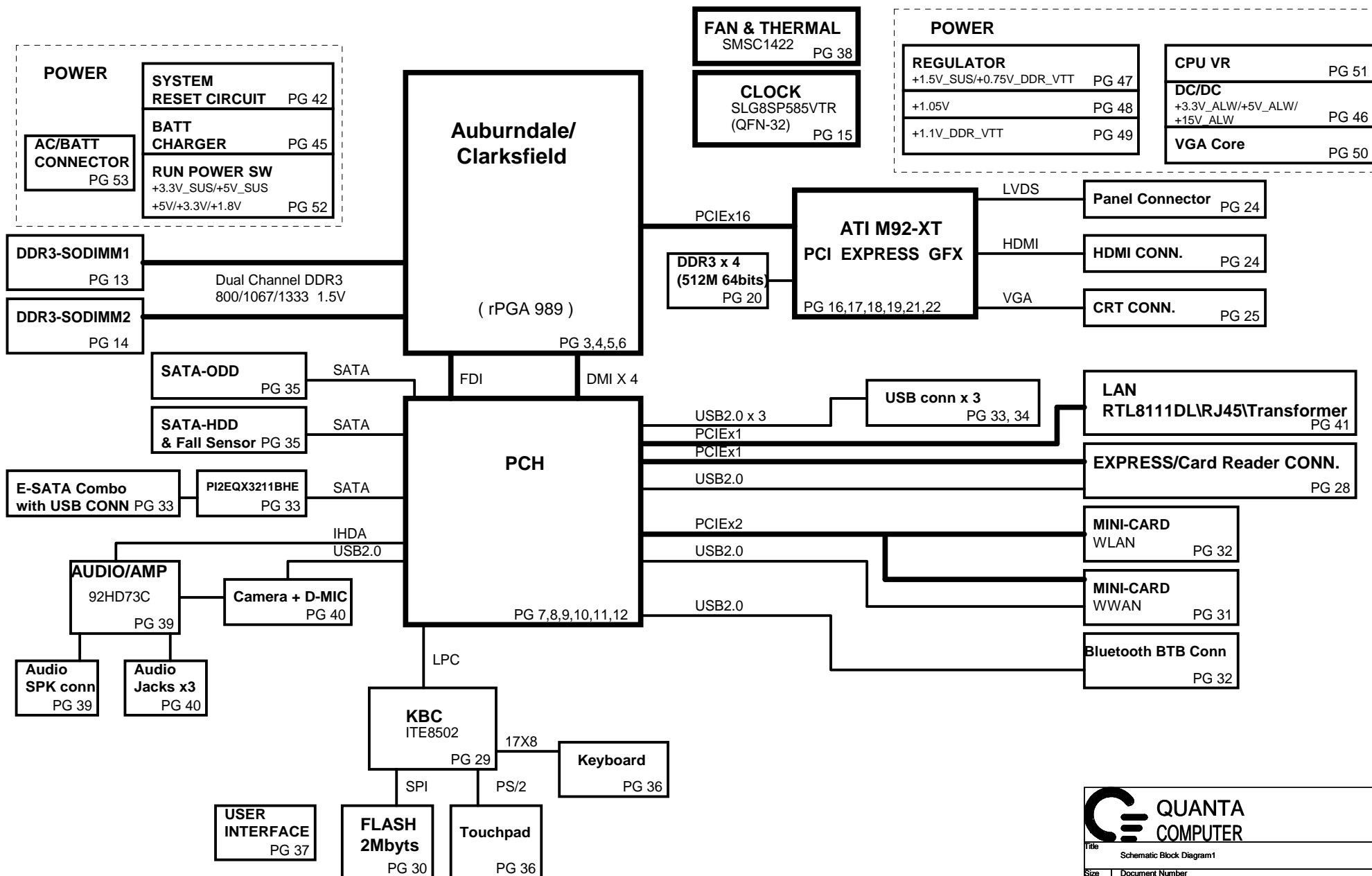









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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	08,29,30,35,36,37,42,44,45,46,47,52,53	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,46,53	LARGE POWER	RUN_ON	S0~S5
+3.3V_LAN	+3.3V	41	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,33,34,35,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,09,10,11,13,14,19,24,26,28,29,37,41,42,44,48,49,50,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.8V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.9V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,59	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,26,44,52	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	CALISTOGA/ICH9 POWER	RUN_ON	
+1.8V_RUN_GFX	+1.25V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,59			
+1.1V_GFX_PCIE	+1.1V	18,50			

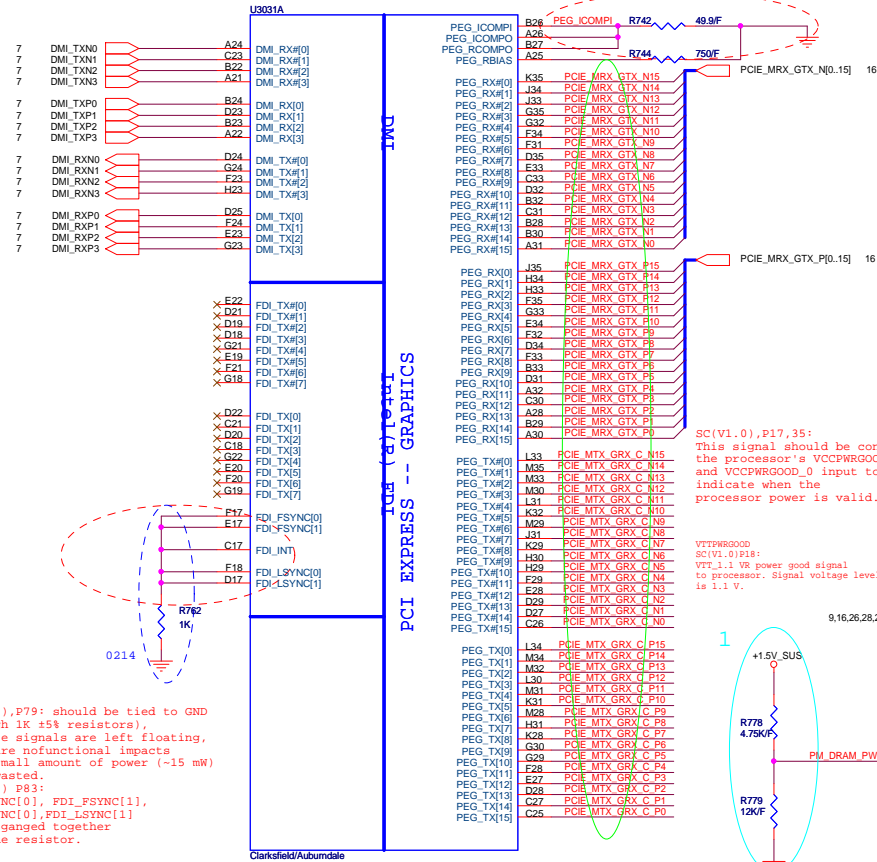
GND PLANE	PAGE	DESCRIPTION
 GND_CHG	46	
 GND_1.05V	47	
 GND_VGA	50	
 GND_SIGNAL	51	
 AGND_DC/DC	52	
 GND	ALL	

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AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

SC(V1.0),P11: Should be shorted at the pins and then routed to one end of the 49.9-Q $\pm 1\%$ resistor, pulled-down to GND on the board.

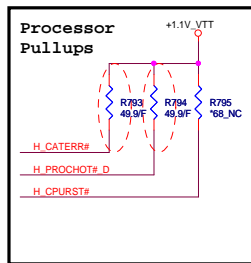


SC(V1.0),P17,35: This signal should be connected to the processor's VCCPWRGOOD_1 and VCCPWRGOOD_0 input to indicate when the processor power is valid.

VTT_PWRGOOD SC(V1.0),P18: VTT_1.1 VR power good signal to processor. Signal voltage level is 1.1 V.

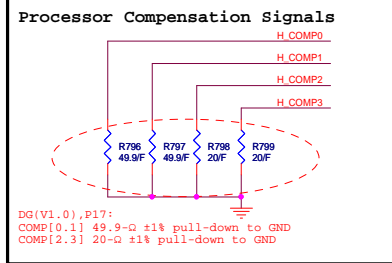
RSTIN# (Doc. # 414074) P10: Need a voltage divider network to scale down from 3.3V (PCH driven) to 1.05V/1.1V (Clarksfield/Auburndale)

SM_DRAMPWROK: DG(V1.0),P31&SC(V1.0),P18: recommend 4.7k- Ω pull-up to DDR3 Power Rail (VDDQ) of +V1.5V and a 12-k Ω pull-down to ground to convert to processor's VTT level. CRB(V1.0) P11: CRB uses a 3.3V (always ON) rail with 2k and 1k combination; CRB Implementation is different for the Calpella Platform Design Guide. Customers to follow the latest Calpella Platform Design Guide for DRAMPWROK implementation.

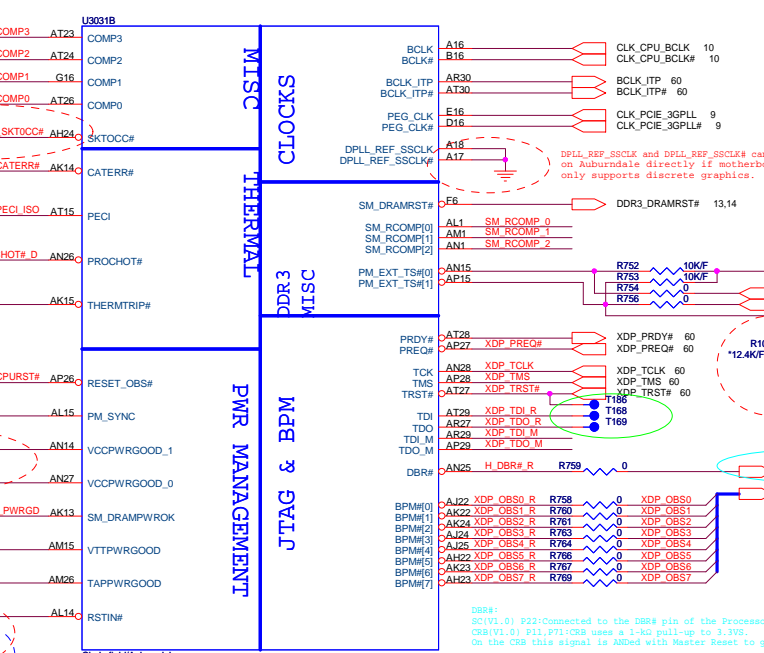


SC(1.0V),P17: H_PROCHOT# use: pull to 68 ohm if it isn't used: pull to 50 ohm

SC(1.0V),P17: 49.9-Q $\pm 1\%$ Pull-Up to the VTT rail (+V1.5V_VTT)



DG(V1.0),P17: COMP[0..1] 49.9-Q $\pm 1\%$ pull-down to GND COMP[2..3] 20-Q $\pm 1\%$ pull-down to GND

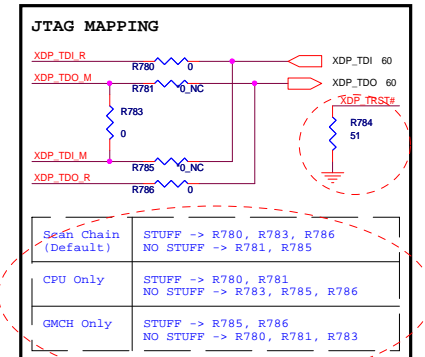
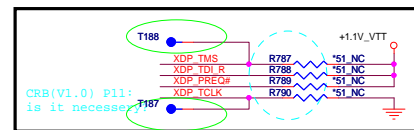
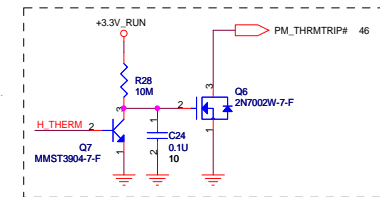


DPLL_REF_SSCLK# and DPLL_REF_SCLK# can be connected to GND on Auburndale directly if motherboard only supports discrete graphics.

CRB(v0.71) P.11

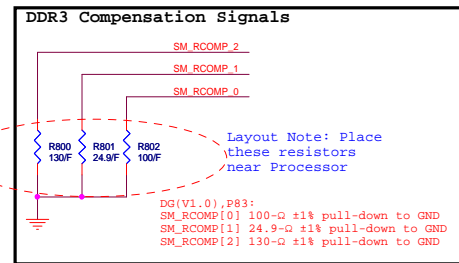
DBR8: SC(V1.0),P22: Connected to the DBR8 pin of the Processor. 50-Q to 5-k Ω pull-up to 3.3V CRB(V1.0) P11: CRB uses a 1-k Ω pull-up to 3.3V. On the CRB this signal is Anded with Master Reset to generate STS_RESET.

DBR8: (Intell feedback) Nothing wrong w/ CRB design. If you want to connect it to PCH directly, make sure pull high to 3.3V (SD) main power.



Scan Chain (Default)	STUFF -> R780, R783, R786 NO STUFF -> R781, R785
CPU Only	STUFF -> R780, R781 NO STUFF -> R783, R785, R786
GMCH Only	STUFF -> R785, R786 NO STUFF -> R780, R781, R783

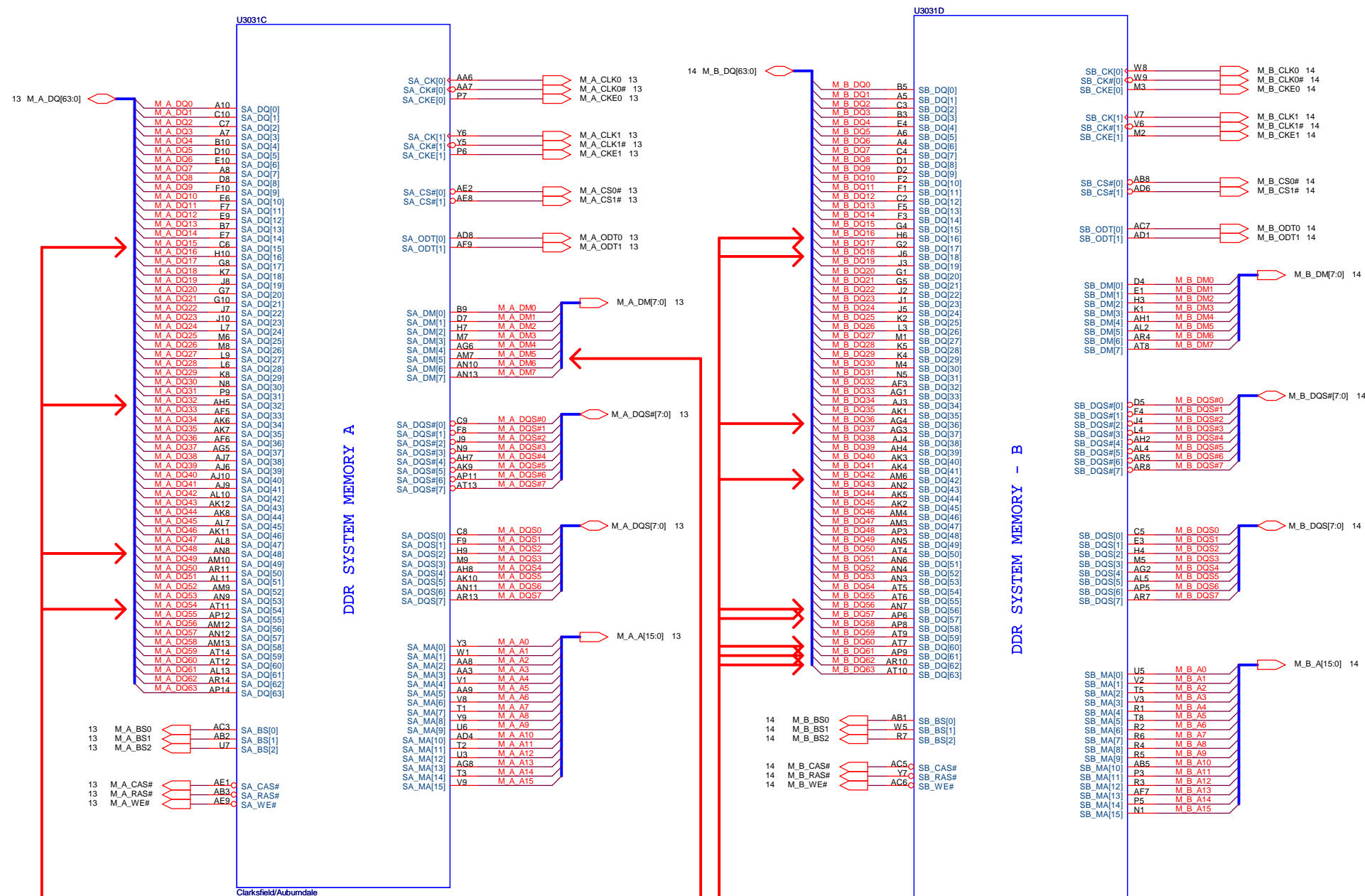
DG(V1.0) table 27: SC(V1.0),P22: should be routed as a single daisy chain to all loads and terminated at the end of the trace. 51-Q $\pm 5\%$ pull down resistor. CRB(V1.0),P11



Layout Note: Place these resistors near Processor

DG(V1.0),P83: SM_RCMP[0] 100-Q $\pm 1\%$ pull-down to GND SM_RCMP[1] 24.9-Q $\pm 1\%$ pull-down to GND SM_RCMP[2] 130-Q $\pm 1\%$ pull-down to GND

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

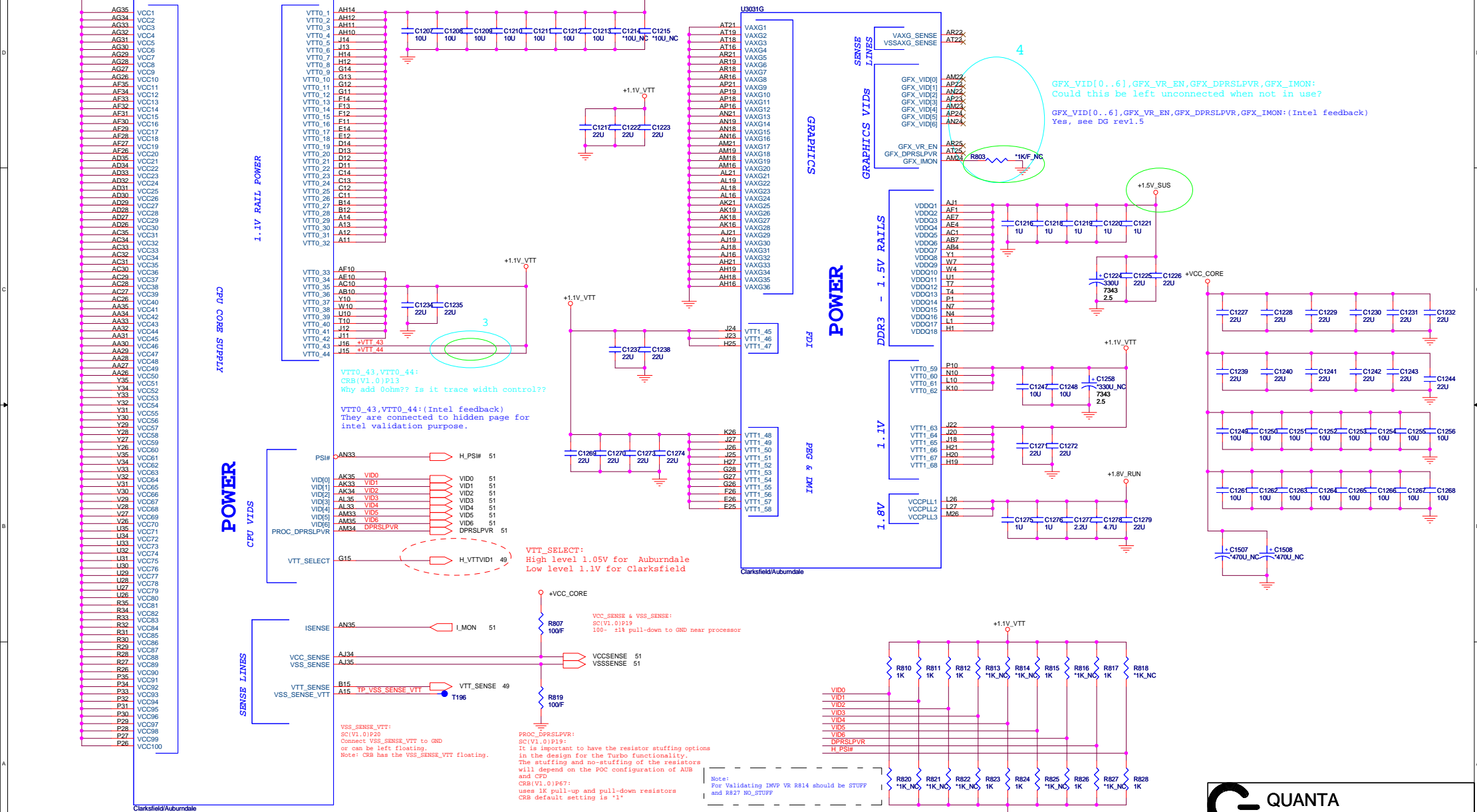


Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals

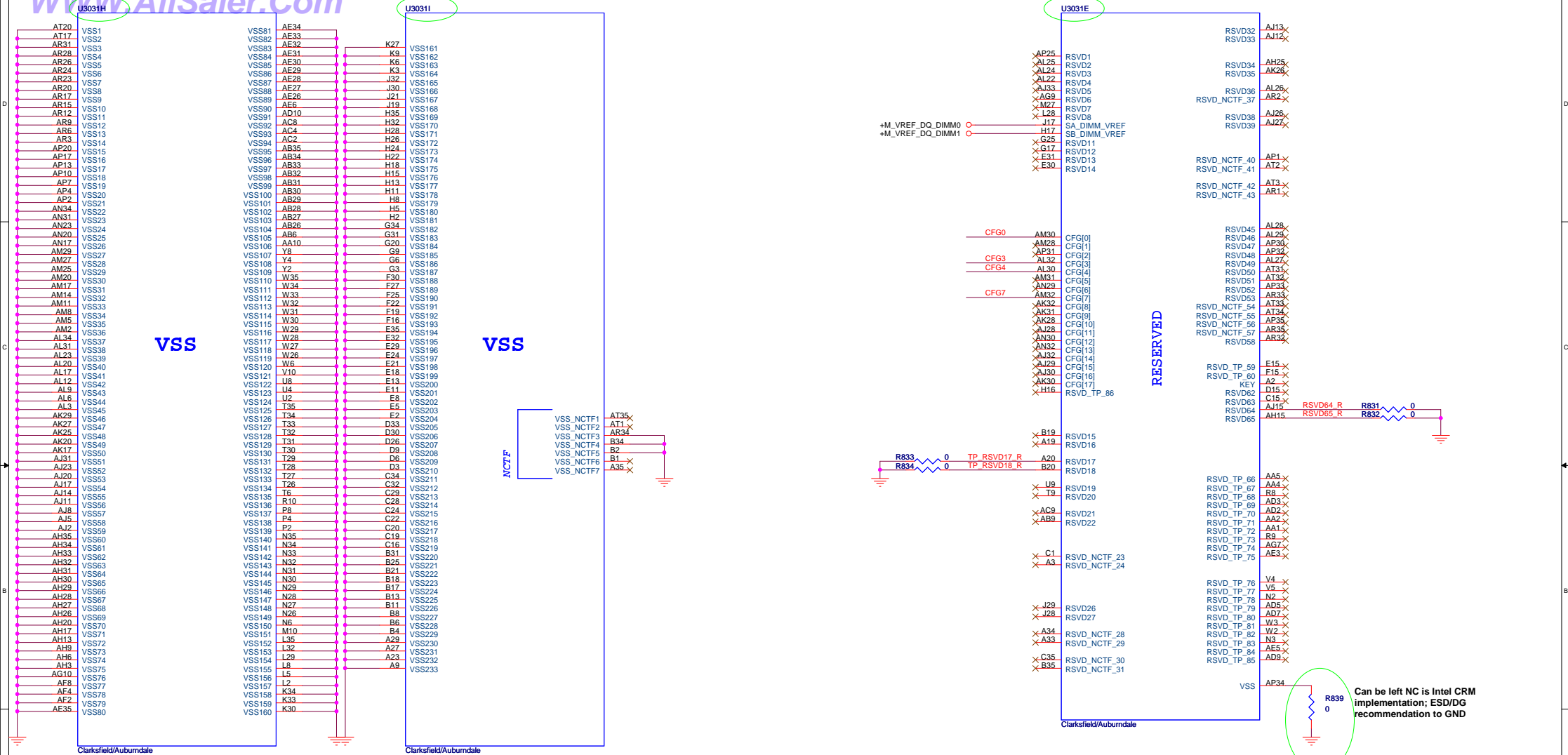


Title			
AUBURNDA 2/4			
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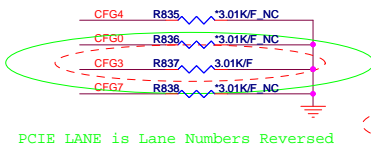


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



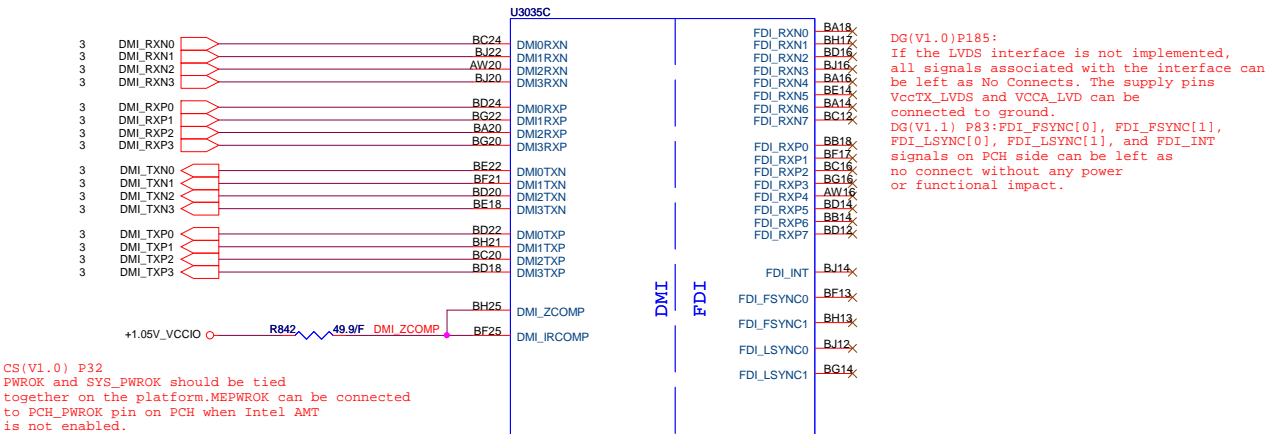
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

**QUANTA
COMPUTER**

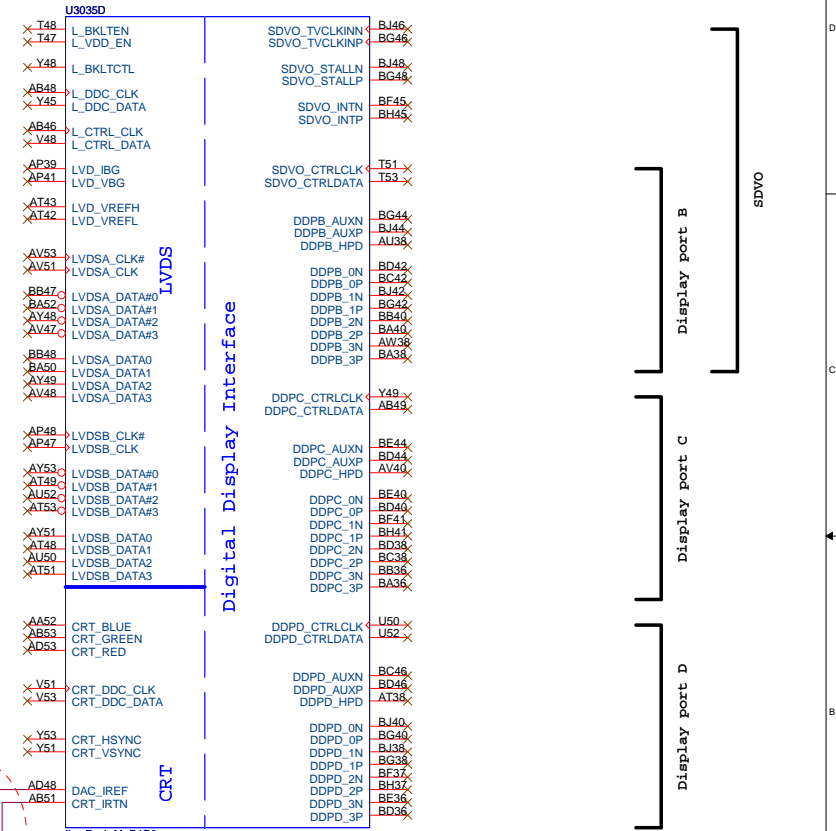
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IBEX PEAK-M (DMI,FDI,GPIO)

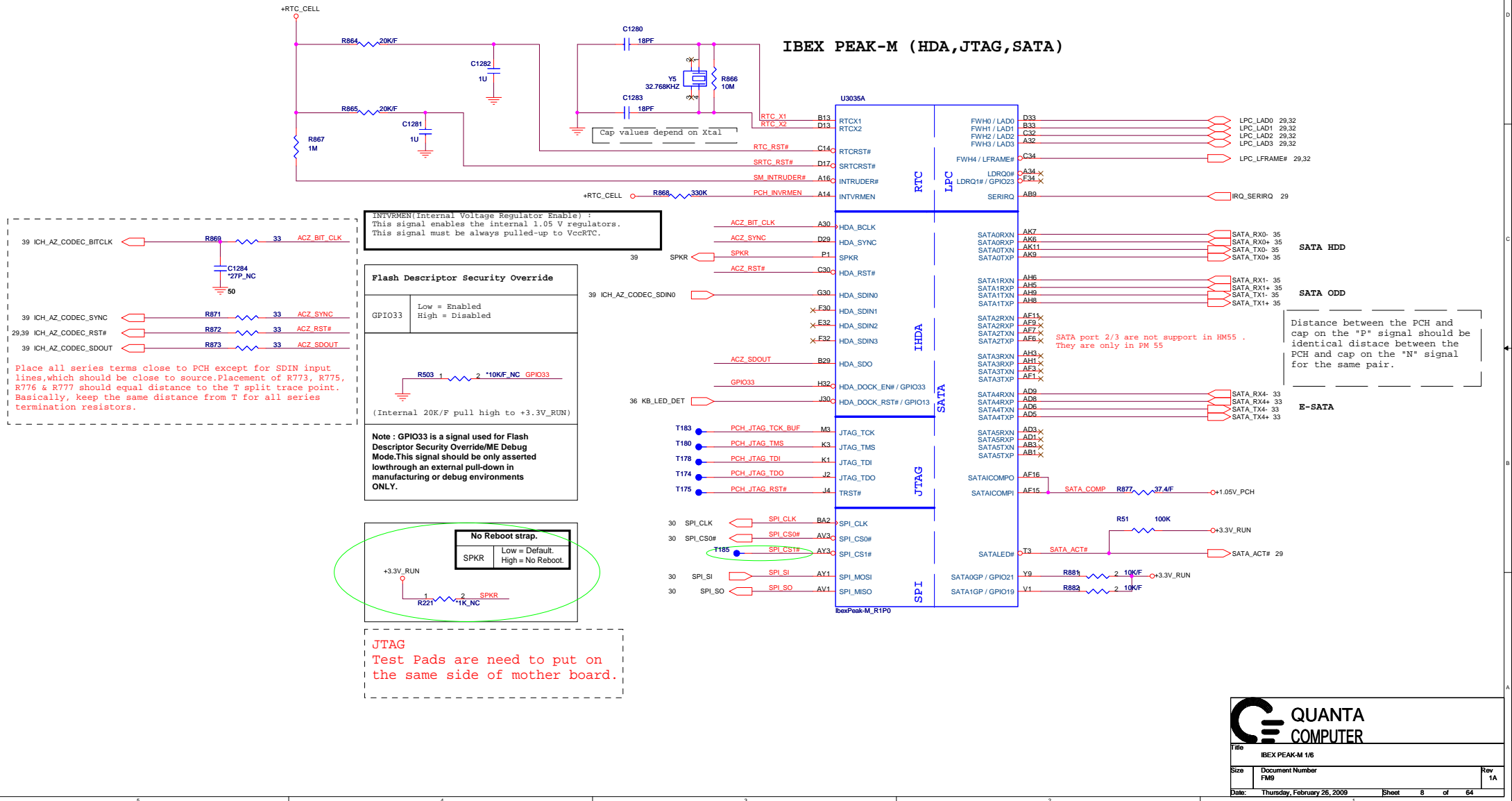
IBEX PEAK-M (LVDS,DDI)



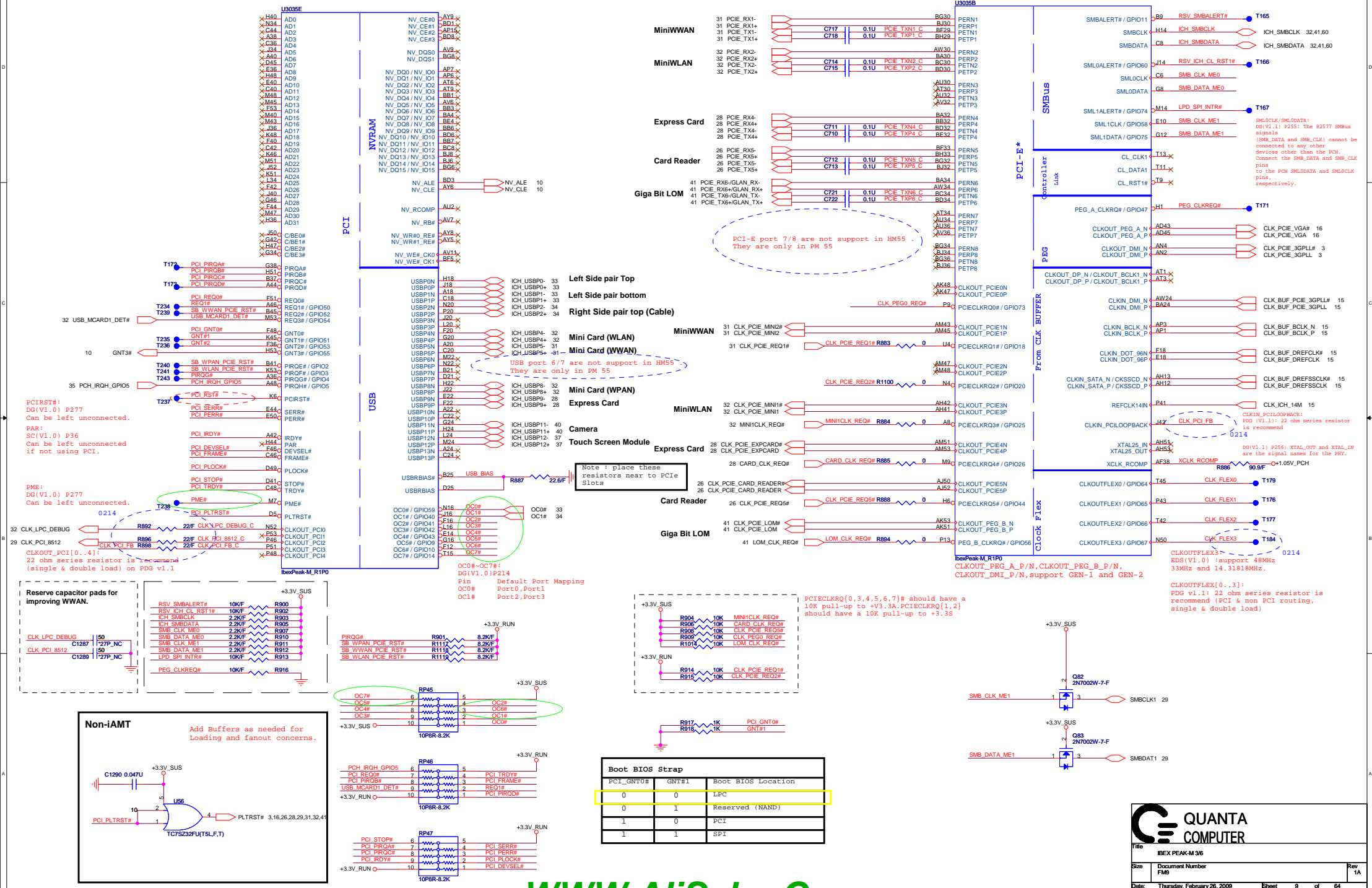
DG(V1.0)P185:
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects. The supply pins VccTX_LVDS and VCCA_LVD can be connected to ground.
DG(V1.1) P83: FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.

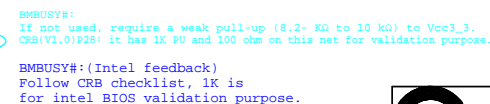
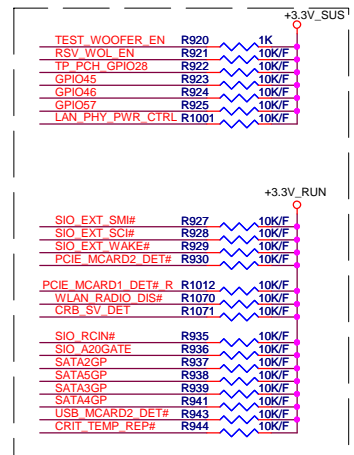


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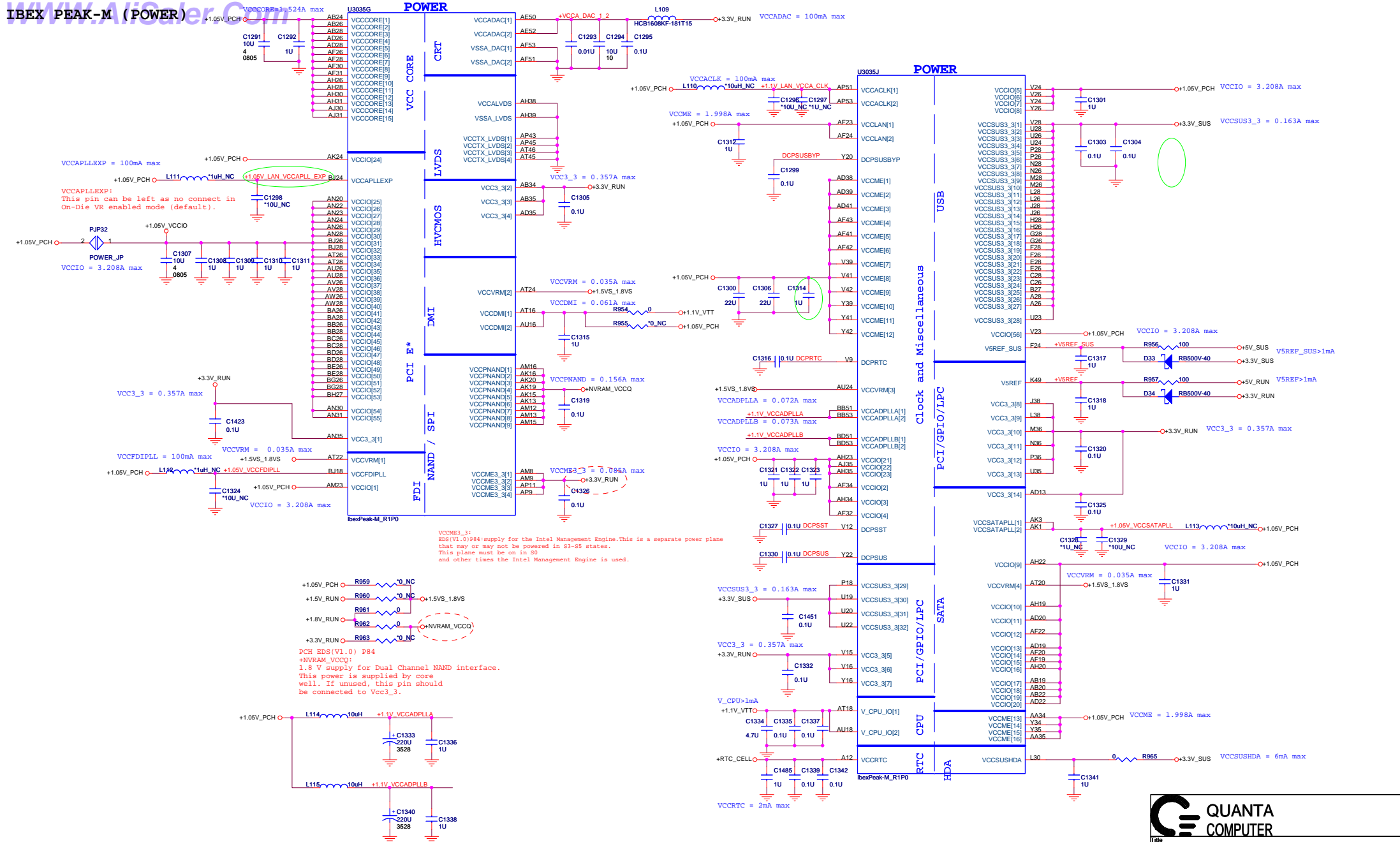
Place TX DC blocking caps close PCH.





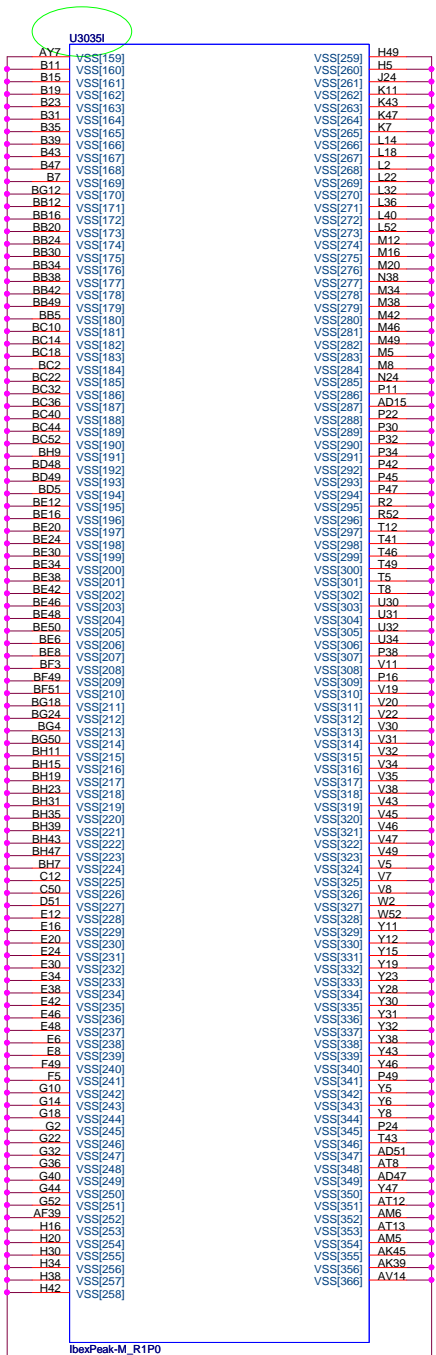
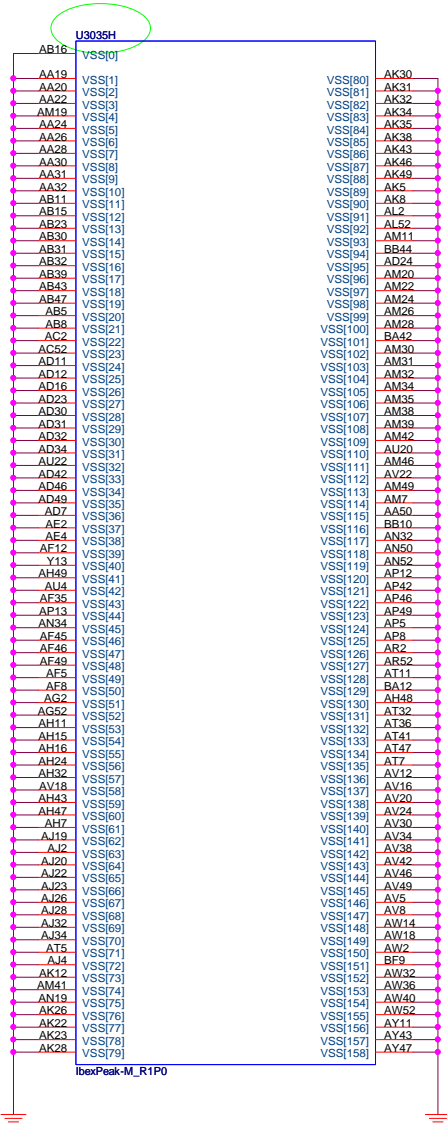
SV_SET_UP	1-X High = Strong (Default)
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Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

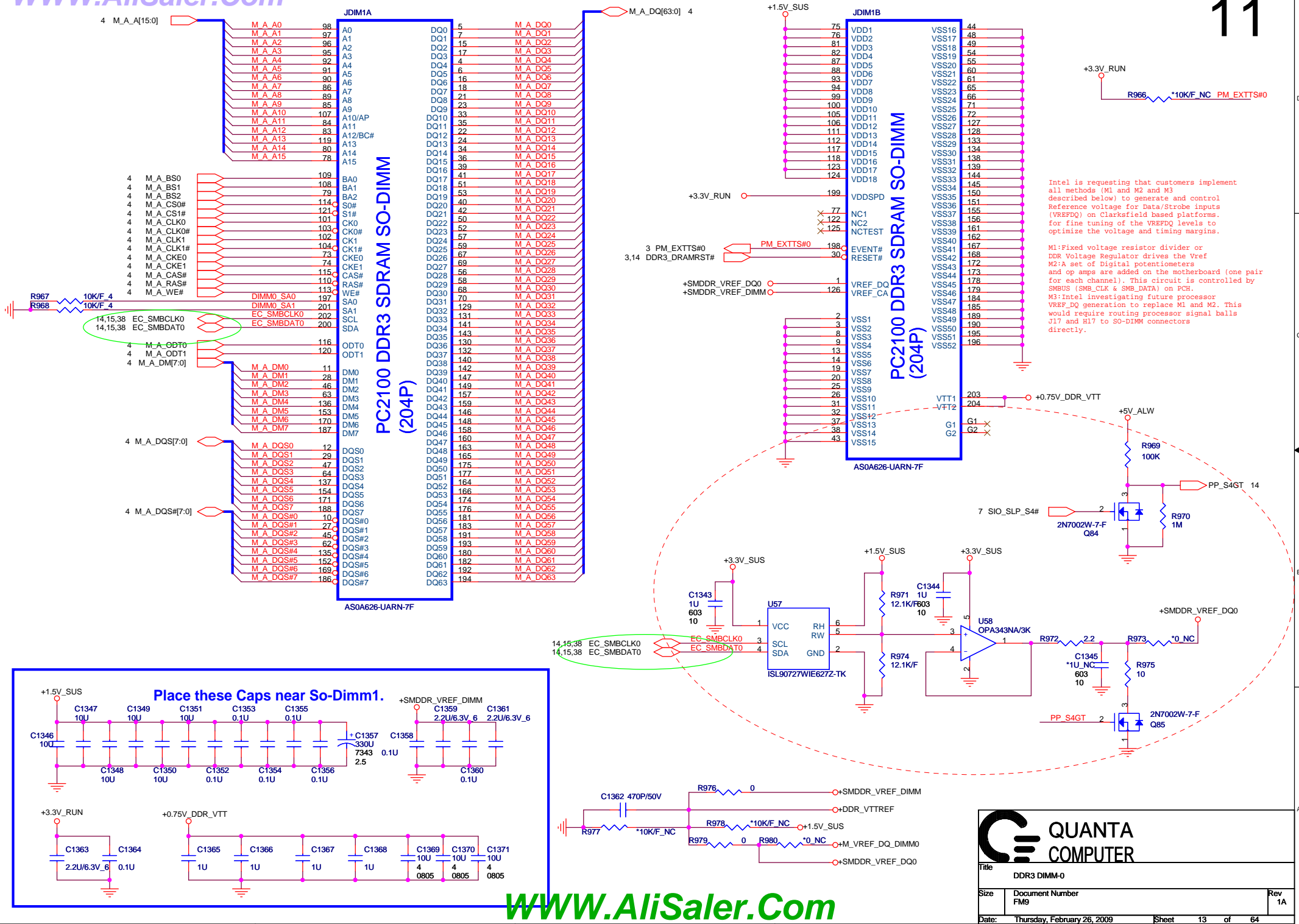


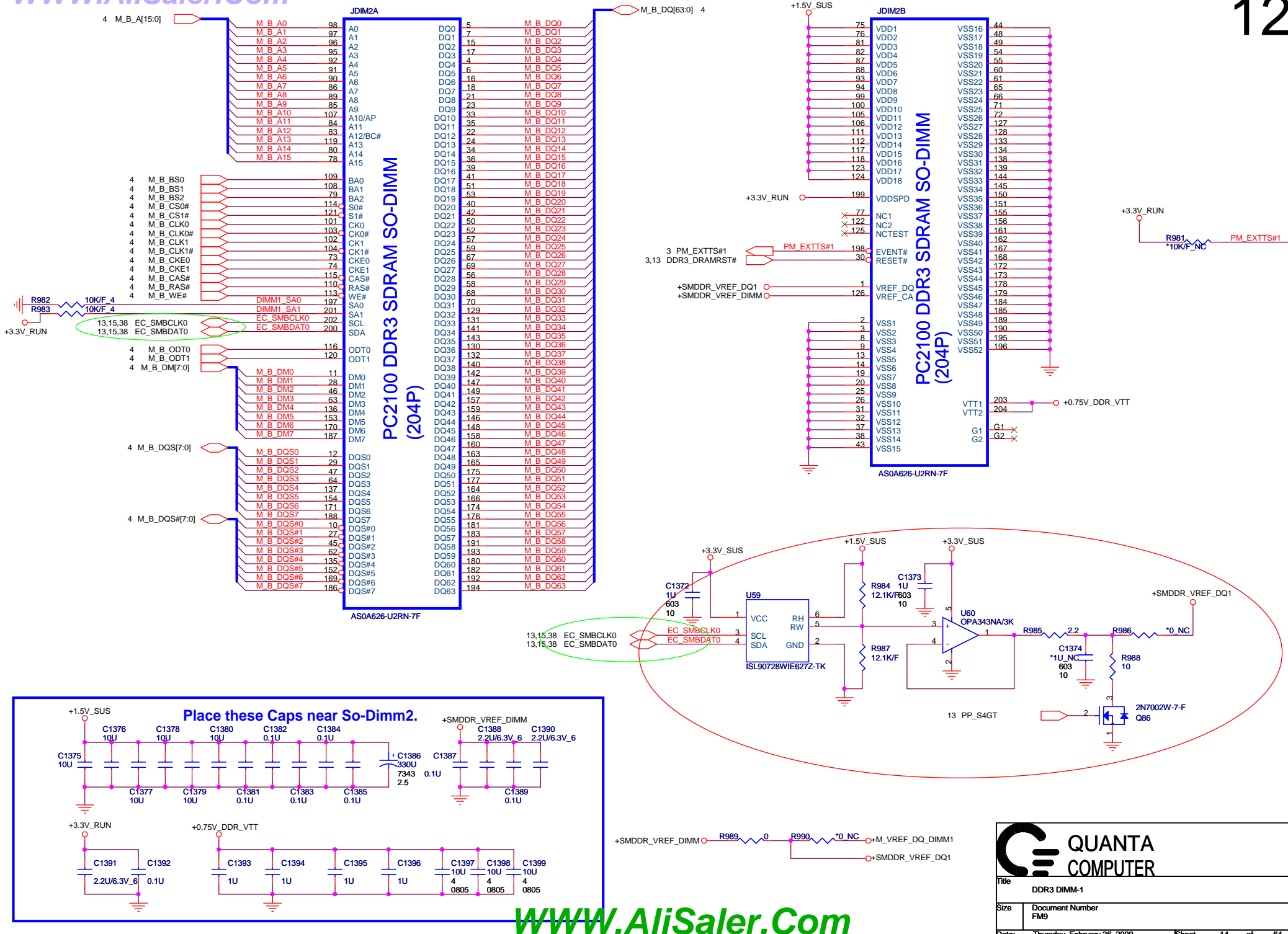
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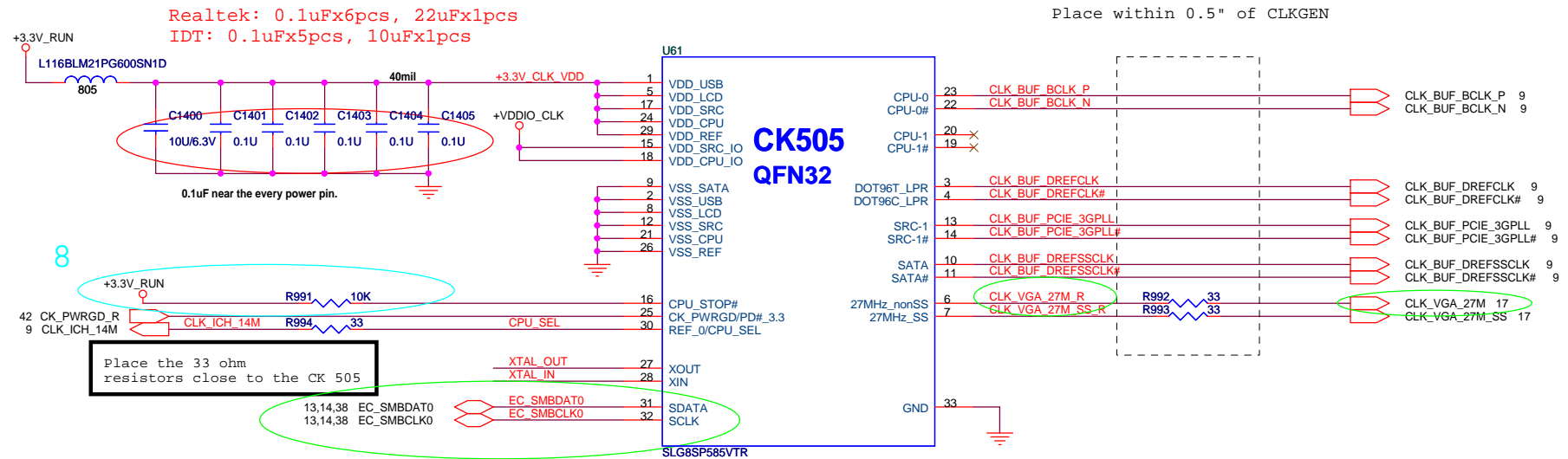
IBEX PEAK-M (GND)



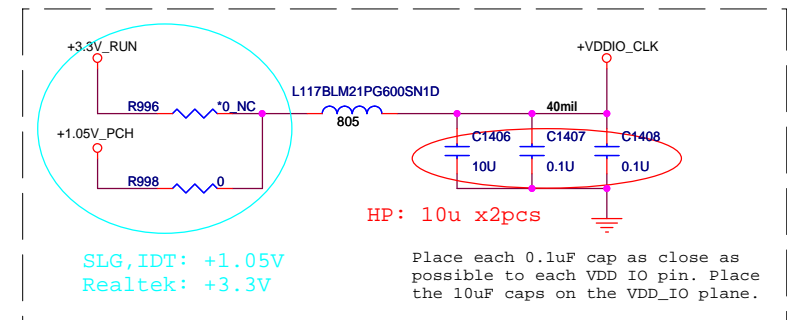
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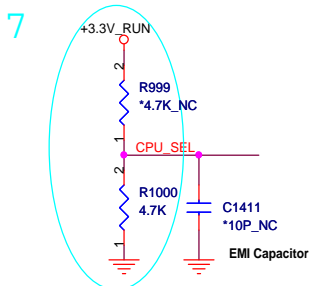


Realtek: 0.1uF x 3 pcs, 22uF x 1 pcs
IDT: 0.1uF x 2 pcs, 10uF x 1 pcs



SLG, IDT: +1.05V
Realtek: +3.3V

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.



PIN	30	CPU_0	CPU_1
0 (default)		133MHz	133MHz
1 (0.7V-1.5V)		100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet (V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet (V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

3 PCIE_MTX_GRX_P0..15] 3 PCIE_MTX_GRX_N0..15]

3 PCIE_MRX_GTX_P0..15] 3 PCIE_MRX_GTX_N0..15]

PCIE_MTX_GRX_P0 AF30 PCIE_RX0P
PCIE_MTX_GRX_N0 AE31 PCIE_RX0N

PCIE_MTX_GRX_P1 AE29 PCIE_RX1P
PCIE_MTX_GRX_N1 AD28 PCIE_RX1N

PCIE_MTX_GRX_P2 AD30 PCIE_RX2P
PCIE_MTX_GRX_N2 AC31 PCIE_RX2N

PCIE_MTX_GRX_P3 AC29 PCIE_RX3P
PCIE_MTX_GRX_N3 AB28 PCIE_RX3N

PCIE_MTX_GRX_P4 AB30 PCIE_RX4P
PCIE_MTX_GRX_N4 AA31 PCIE_RX4N

PCIE_MTX_GRX_P5 AA29 PCIE_RX5P
PCIE_MTX_GRX_N5 Y28 PCIE_RX5N

PCIE_MTX_GRX_P6 Y30 PCIE_RX6P
PCIE_MTX_GRX_N6 W31 PCIE_RX6N

PCIE_MTX_GRX_P7 W28 PCIE_RX7P
PCIE_MTX_GRX_N7 V28 PCIE_RX7N

PCIE_MTX_GRX_P8 V30 PCIE_RX8P
PCIE_MTX_GRX_N8 U31 PCIE_RX8N

PCIE_MTX_GRX_P9 U29 PCIE_RX9P
PCIE_MTX_GRX_N9 T28 PCIE_RX9N

PCIE_MTX_GRX_P10 T30 PCIE_RX10P
PCIE_MTX_GRX_N10 R31 PCIE_RX10N

PCIE_MTX_GRX_P11 R29 PCIE_RX11P
PCIE_MTX_GRX_N11 P28 PCIE_RX11N

PCIE_MTX_GRX_P12 P30 PCIE_RX12P
PCIE_MTX_GRX_N12 N31 PCIE_RX12N

PCIE_MTX_GRX_P13 N29 PCIE_RX13P
PCIE_MTX_GRX_N13 M28 PCIE_RX13N

PCIE_MTX_GRX_P14 M30 PCIE_RX14P
PCIE_MTX_GRX_N14 L31 PCIE_RX14N

PCIE_MTX_GRX_P15 L29 PCIE_RX15P
PCIE_MTX_GRX_N15 K30 PCIE_RX15N

PCIE_TX0P AH30 PCIE_MRX_GTX_C_P0
PCIE_TX0N AG31 PCIE_MRX_GTX_C_N0

PCIE_TX1P AG29 PCIE_MRX_GTX_C_P1
PCIE_TX1N AF28 PCIE_MRX_GTX_C_N1

PCIE_TX2P AF27 PCIE_MRX_GTX_C_P2
PCIE_TX2N AF26 PCIE_MRX_GTX_C_N2

PCIE_TX3P AD27 PCIE_MRX_GTX_C_P3
PCIE_TX3N AD26 PCIE_MRX_GTX_C_N3

PCIE_TX4P AC25 PCIE_MRX_GTX_C_P4
PCIE_TX4N AB25 PCIE_MRX_GTX_C_N4

PCIE_TX5P Y23 PCIE_MRX_GTX_C_P5
PCIE_TX5N Y24 PCIE_MRX_GTX_C_N5

PCIE_TX6P AB27 PCIE_MRX_GTX_C_P6
PCIE_TX6N AB26 PCIE_MRX_GTX_C_N6

PCIE_TX7P Y27 PCIE_MRX_GTX_C_P7
PCIE_TX7N Y26 PCIE_MRX_GTX_C_N7

PCIE_TX8P W24 PCIE_MRX_GTX_C_P8
PCIE_TX8N W23 PCIE_MRX_GTX_C_N8

PCIE_TX9P V27 PCIE_MRX_GTX_C_P9
PCIE_TX9N U26 PCIE_MRX_GTX_C_N9

PCIE_TX10P U24 PCIE_MRX_GTX_C_P10
PCIE_TX10N U23 PCIE_MRX_GTX_C_N10

PCIE_TX11P T26 PCIE_MRX_GTX_C_P11
PCIE_TX11N T27 PCIE_MRX_GTX_C_N11

PCIE_TX12P T24 PCIE_MRX_GTX_C_P12
PCIE_TX12N T23 PCIE_MRX_GTX_C_N12

PCIE_TX13P P27 PCIE_MRX_GTX_C_P13
PCIE_TX13N P26 PCIE_MRX_GTX_C_N13

PCIE_TX14P P24 PCIE_MRX_GTX_C_P14
PCIE_TX14N P23 PCIE_MRX_GTX_C_N14

PCIE_TX15P M27 PCIE_MRX_GTX_C_P15
PCIE_TX15N M26 PCIE_MRX_GTX_C_N15

PCIE_MRX_GTX_P0 0.1U 2 1 C814 10 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C815 10 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C816 10 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C817 10 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C818 10 PCIE_MRX_GTX_C_P4
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PCIE_MRX_GTX_P6 0.1U 2 1 C820 10 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C821 10 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C822 10 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C823 10 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C824 10 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C825 10 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C826 10 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C827 10 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C828 10 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C829 10 PCIE_MRX_GTX_C_P15

PCIE_MRX_GTX_N0 0.1U 2 1 C830 10 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C831 10 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C832 10 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C833 10 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C834 10 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C835 10 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C836 10 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C837 10 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C838 10 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C839 10 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C840 10 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C841 10 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C842 10 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C843 10 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C844 10 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U 2 1 C845 10 PCIE_MRX_GTX_C_N15

100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted

9 CLK_PCIE_VGA AK30 PCIE_REFCLKP
9 CLK_PCIE_VGA# AK32 PCIE_REFCLKN

9,26,28,29,31,32,41 PLTRST# A27 PERSTB

M92-S2M92-XT

M92-S2 XT AJ072800T04 100-CG1675(216-0728004)
M92-S2 AJ072800T03 100-CG1643(216-0728003)

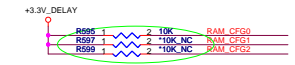
(1.1V)
+PCIE_VDDC

AA22 PCIE_CALRN 2.0K R591
Y22 PCIE_CALRP 1.27K R592

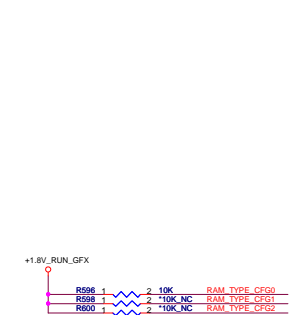
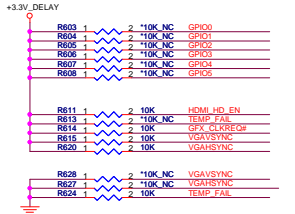


Title			VGA-M92-XT (PCIe)
Size	Document Number	Rev	
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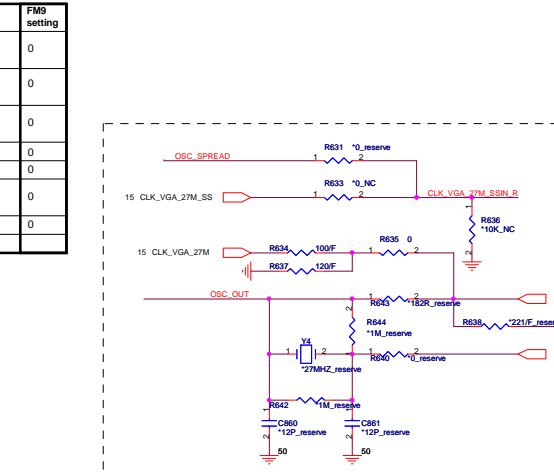
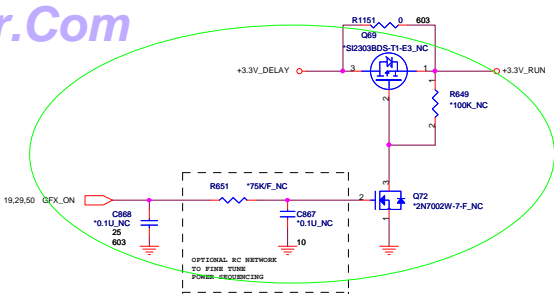
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0	0
256MB	0	0	1	1
64MB	0	1	0	0
512MB	1	0	0	0



GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FW0 setting
GPIO0	GPIO0 - TX_PWRD_EN (Transmitter Power Savings Enable) 0: 50% Tx output swing (Default setting for mobile mode) 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2 - BIF_GEN2_EN (5.0 Gb/s Enable) 0: Default (Driver Controlled Gen2) 1: Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0: Battery saving mode = 0.9 V 1: AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0

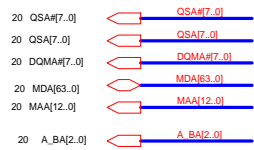


Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 level PN
800MHz	0	0	1	AKD5LG0T502		K4W1G1646B-HC12	
512MB(64M*16) Samsung	0	0	1	AKD5LG0T502		K4W1G1646B-HC12	
800MHz	0	1	0	AKD5L2GTW00		H5TQ1G63BFR-12C	
512MB(64M*16) Hynix	0	1	0	AKD5L2GTW00		H5TQ1G63BFR-12C	

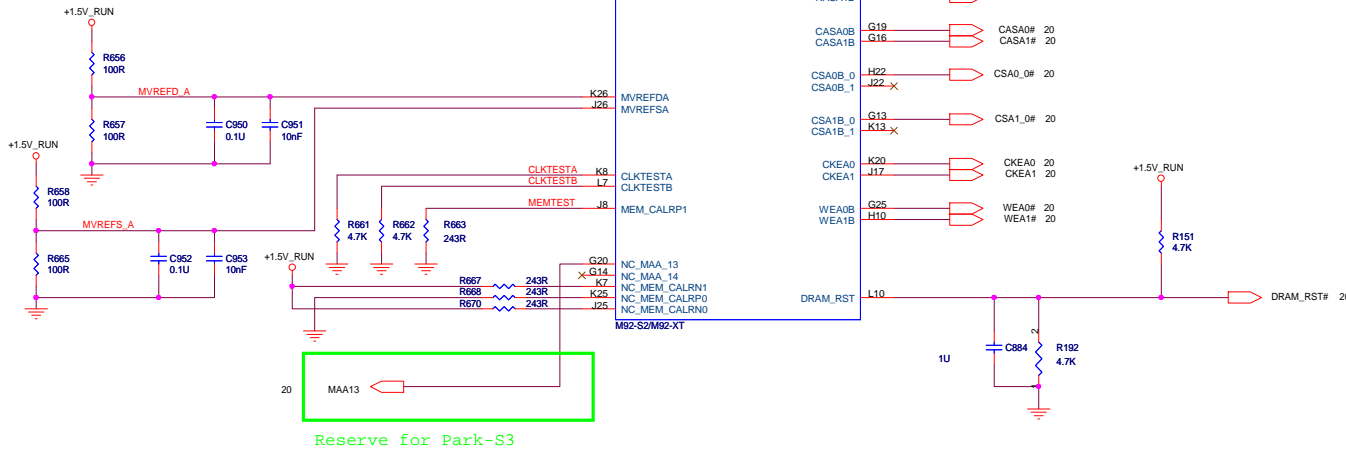


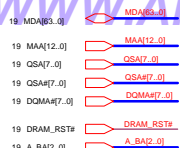


MEMORY INTERFACE

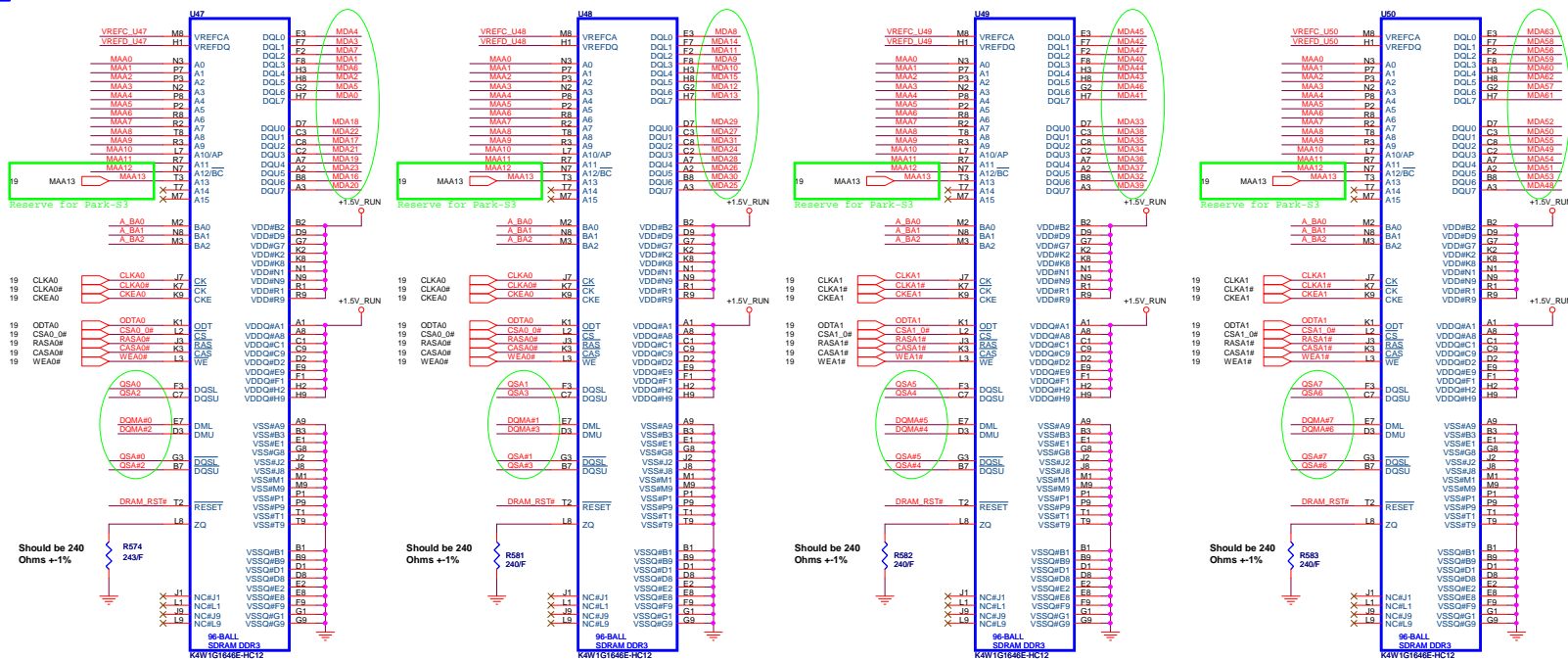


DIVIDER RESISTORS	DDR3
MVREF TO 1.5V	100R
MVREF TO GND	100R

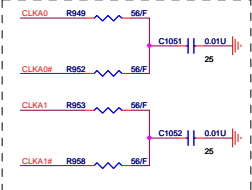




DDR3



Placement has to be close to VRAM

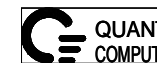
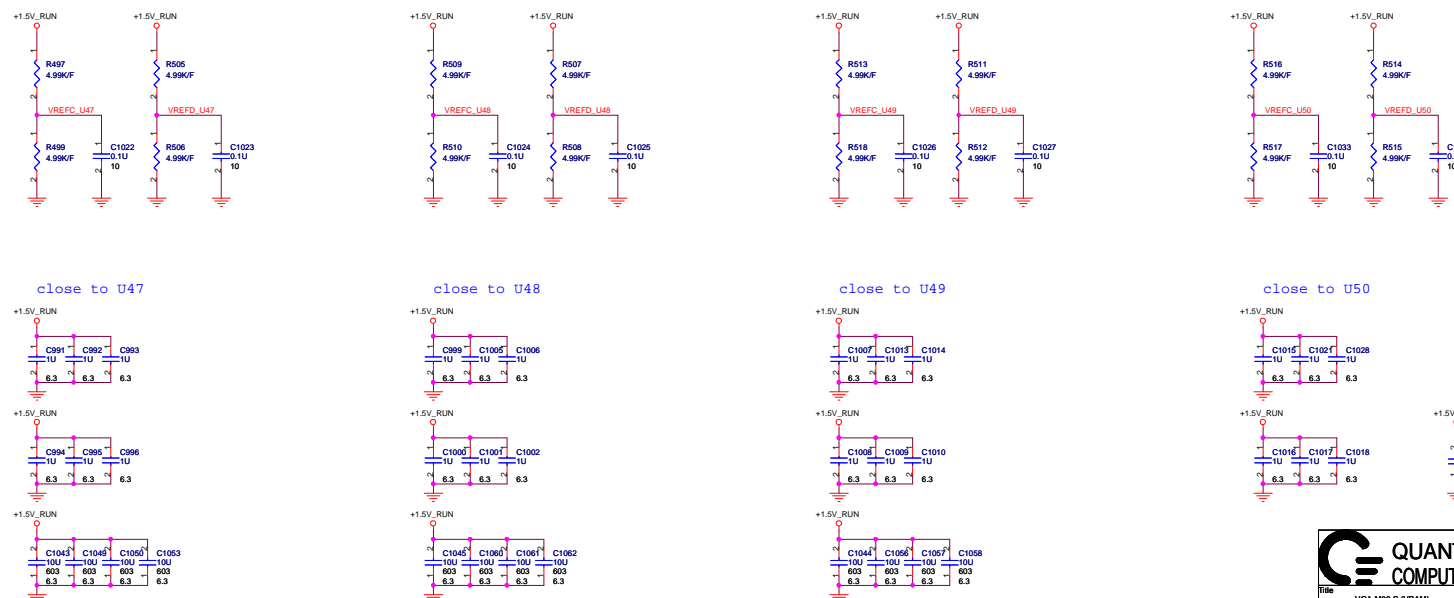


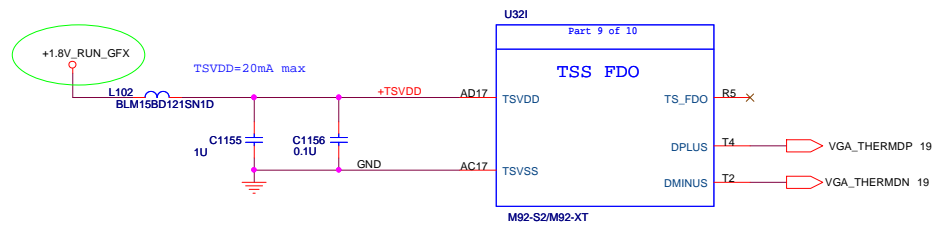
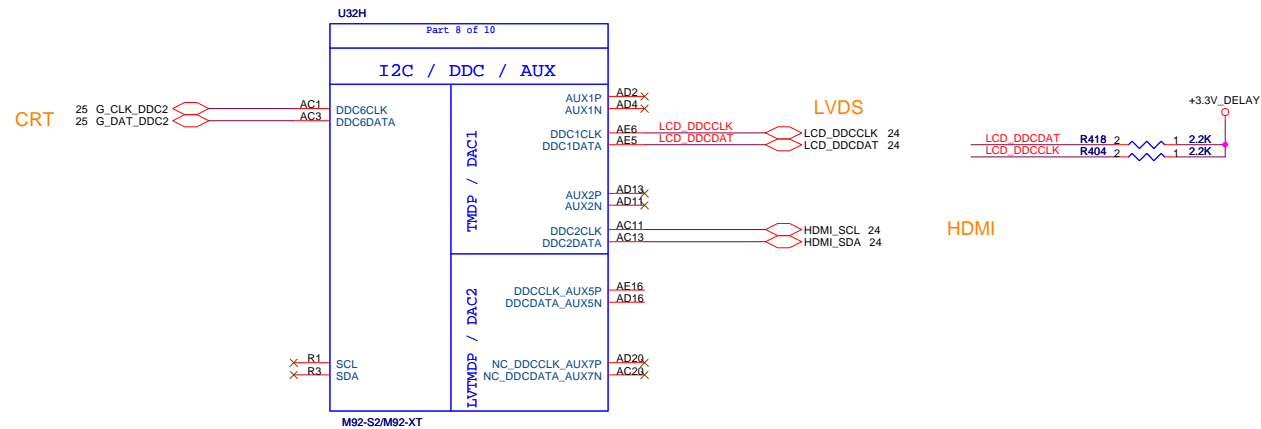
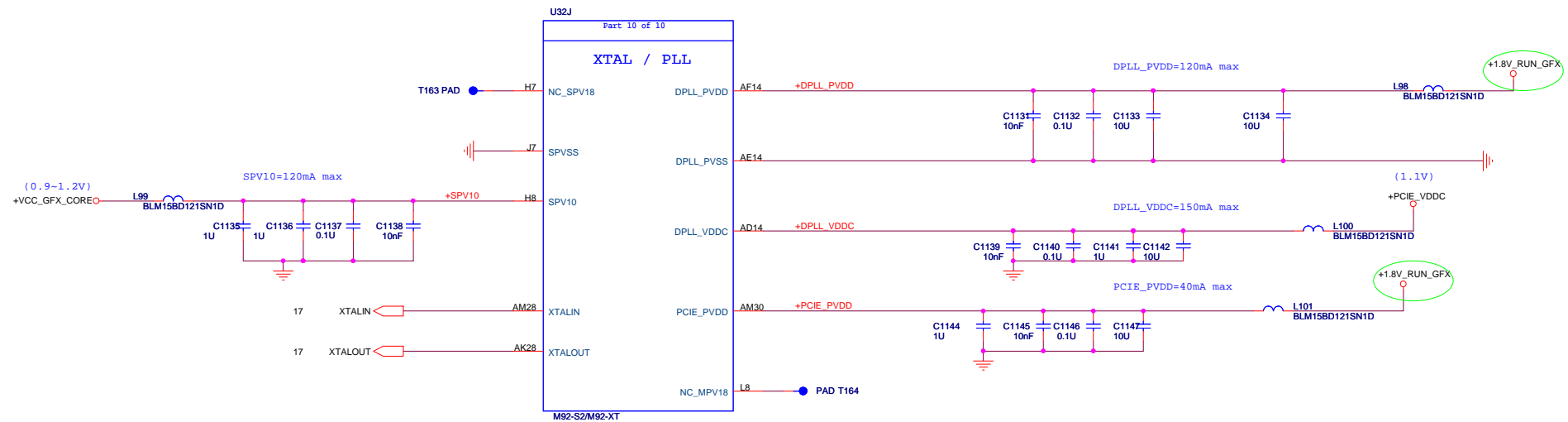
close to U47

close to U48

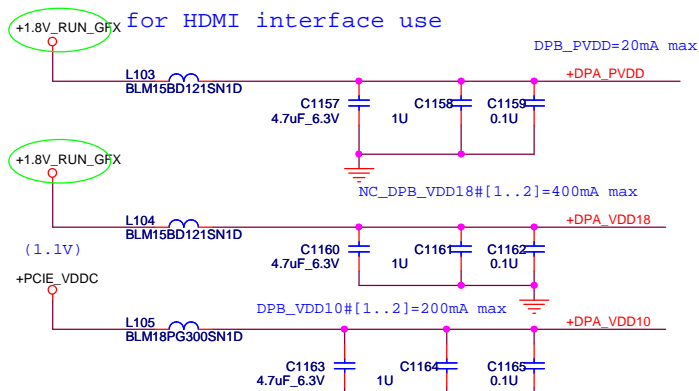
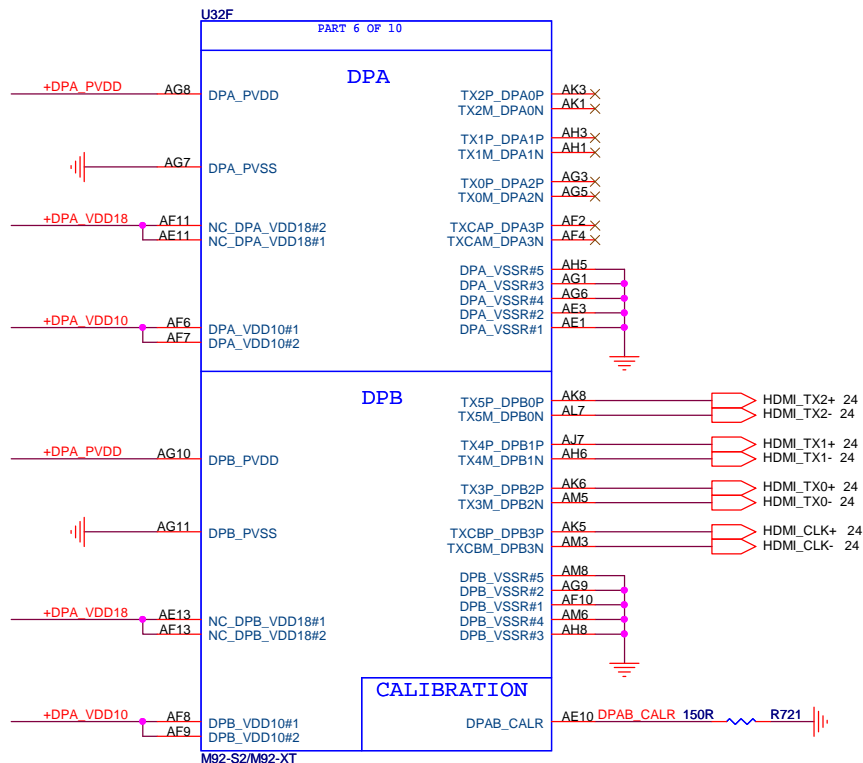
close to U4!

close to U5

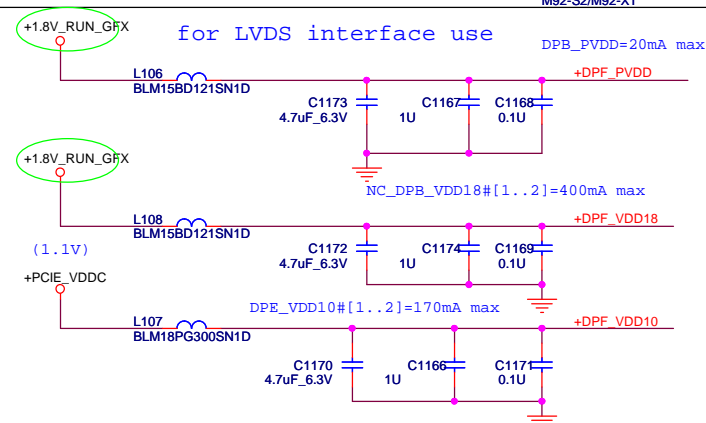
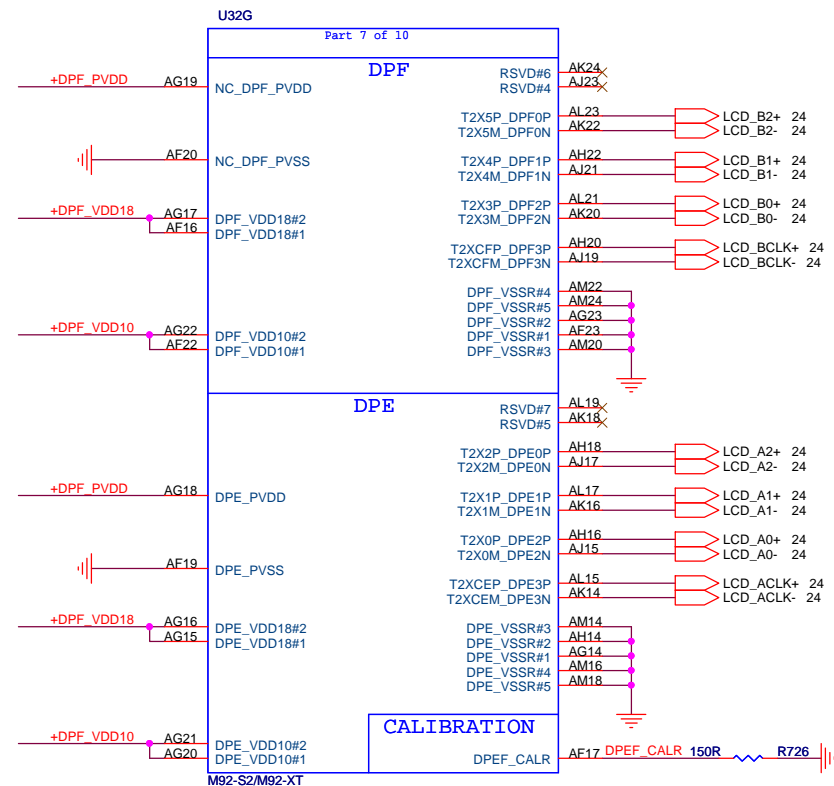




TMDP(HDMI) INTERFACE



LVDS INTERFACE




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D

C

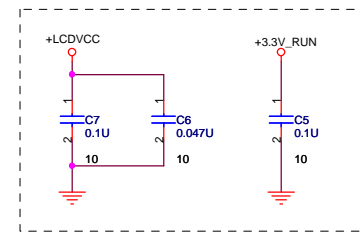
B

A



QUANTA
COMPUTER

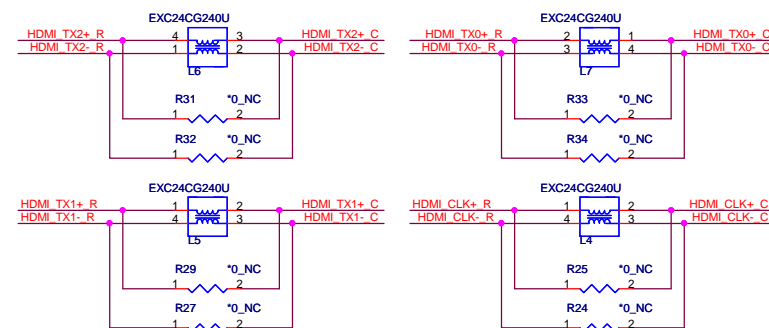
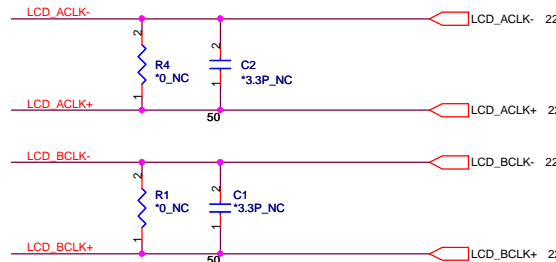
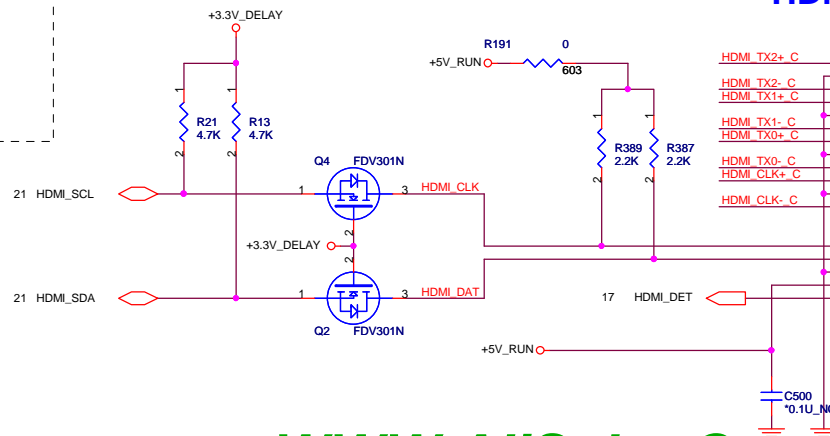
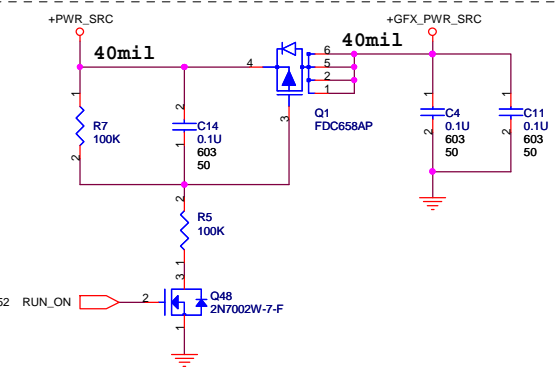
File		
VGA-M82-S (PCIe)		
Size	Document Number	Rev
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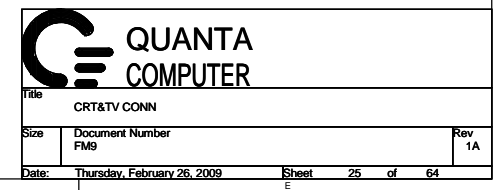
Adress : A9H --Contrast
AAH --Backlight

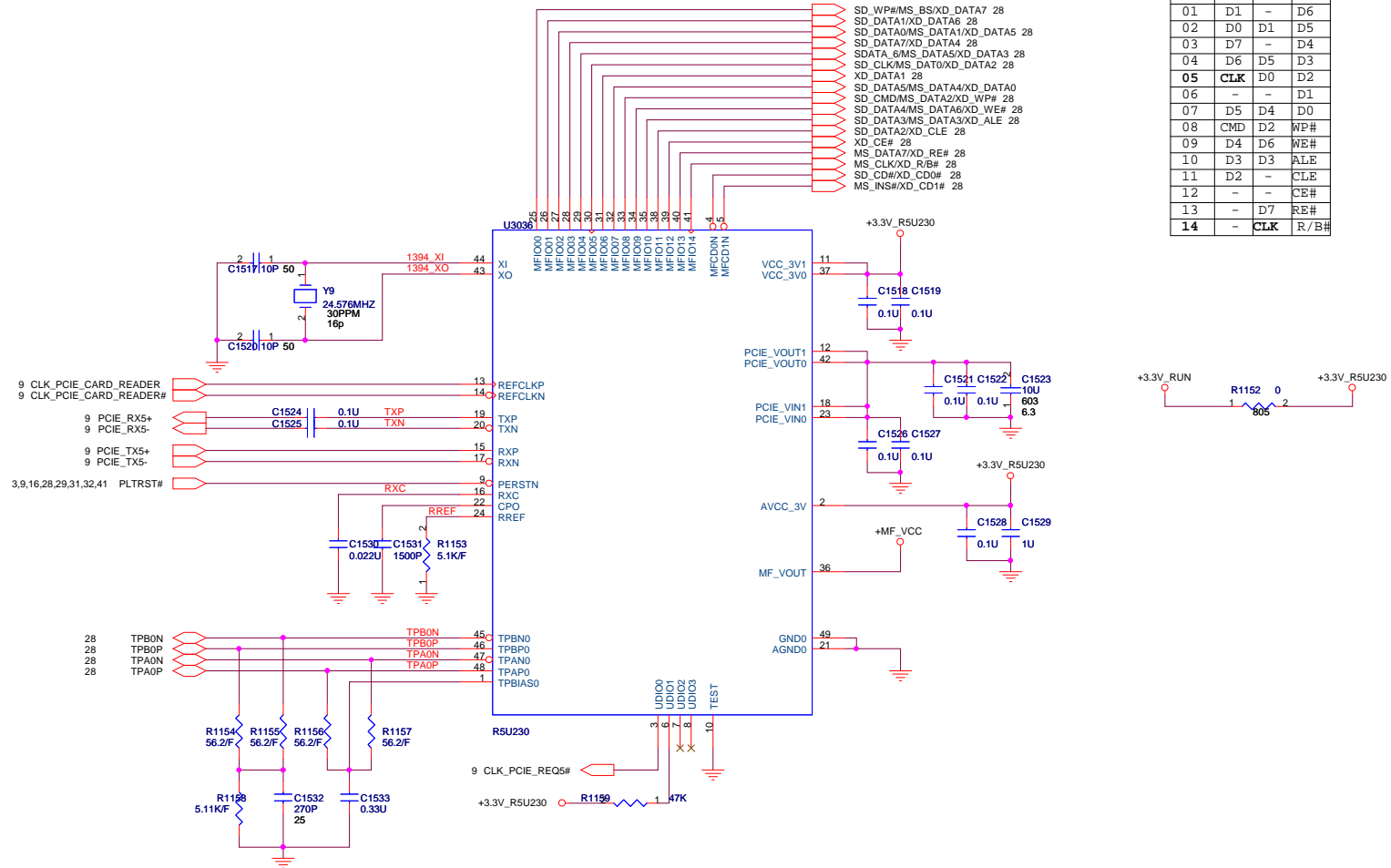


LCD B0-	C16	1	2	*3.3P NC	50	LCD B0+
LCD B1-	C10	1	2	*3.3P NC	50	LCD B1+
LCD B2-	C15	1	2	*3.3P NC	50	LCD B2+
LCD A0-	C13	1	2	*3.3P NC	50	LCD A0+
LCD A1-	C12	1	2	*3.3P NC	50	LCD A1+
LCD A2-	C3	1	2	*3.3P NC	50	LCD A2+

[illegible]

22	HDMI_TX2+		C25	0.1U/10V/X7R	HDMI_TX2+_R
22	HDMI_TX2-		C26	0.1U/10V/X7R	HDMI_TX2-_R
22	HDMI_TX1+		C23	0.1U/10V/X7R	HDMI_TX1+_R
22	HDMI_TX1-		C22	0.1U/10V/X7R	HDMI_TX1-_R
22	HDMI_TX0+		C27	0.1U/10V/X7R	HDMI_TX0+_R
22	HDMI_TX0-		C30	0.1U/10V/X7R	HDMI_TX0-_R
22	HDMI_CLK+		C21	0.1U/10V/X7R	HDMI_CLK+_R
22	HDMI_CLK-		C20	0.1U/10V/X7R	HDMI_CLK-_R





MFIO Pin Assignment Table


MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	CLK	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WE#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	CLK	R/B#



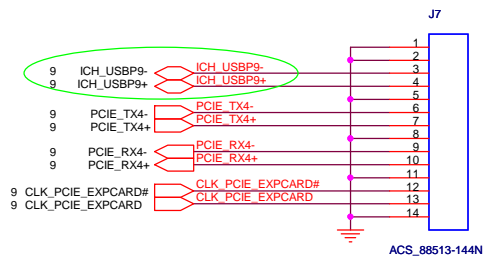
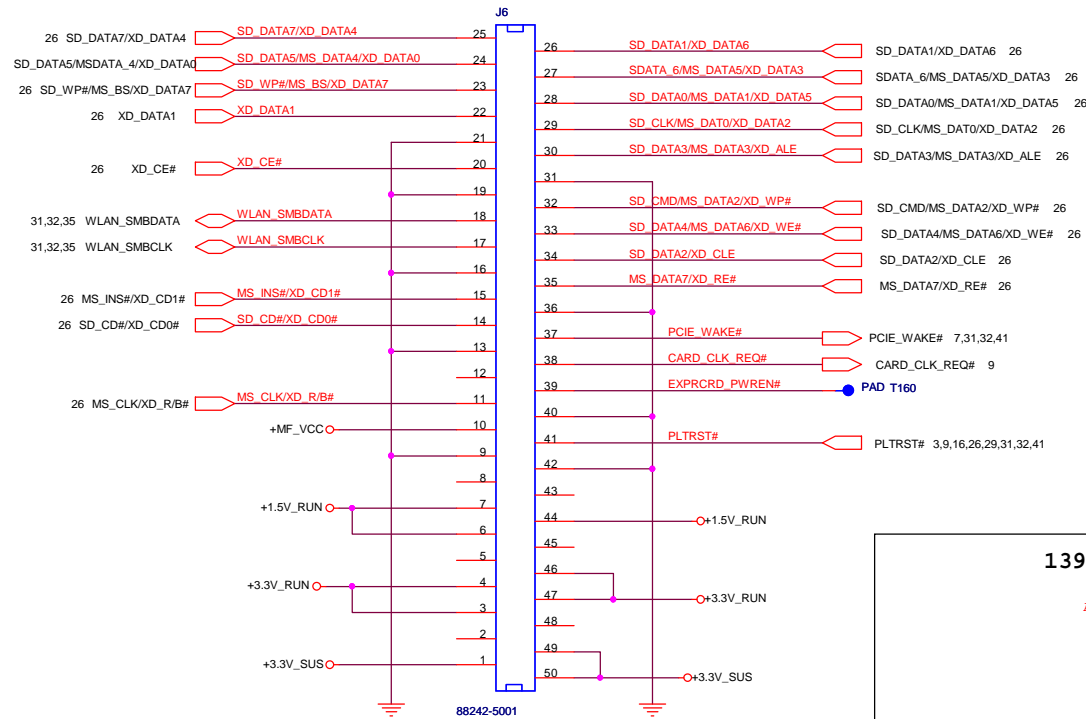
5 IN 1 CONTROLLER

Size Document Number
FM9

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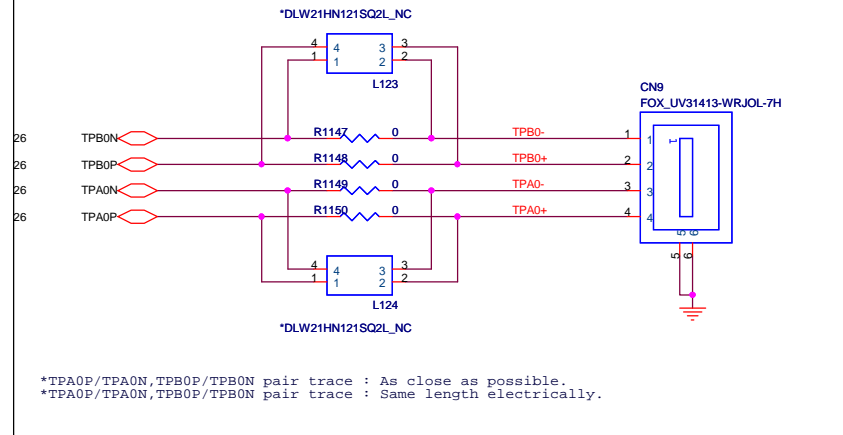
			QUANTA COMPUTER		
Title IEEE 1394					
Size	Document Number FM9				Rev 1A
Date:	Thursday, February 26, 2009		Sheet	27	of 64

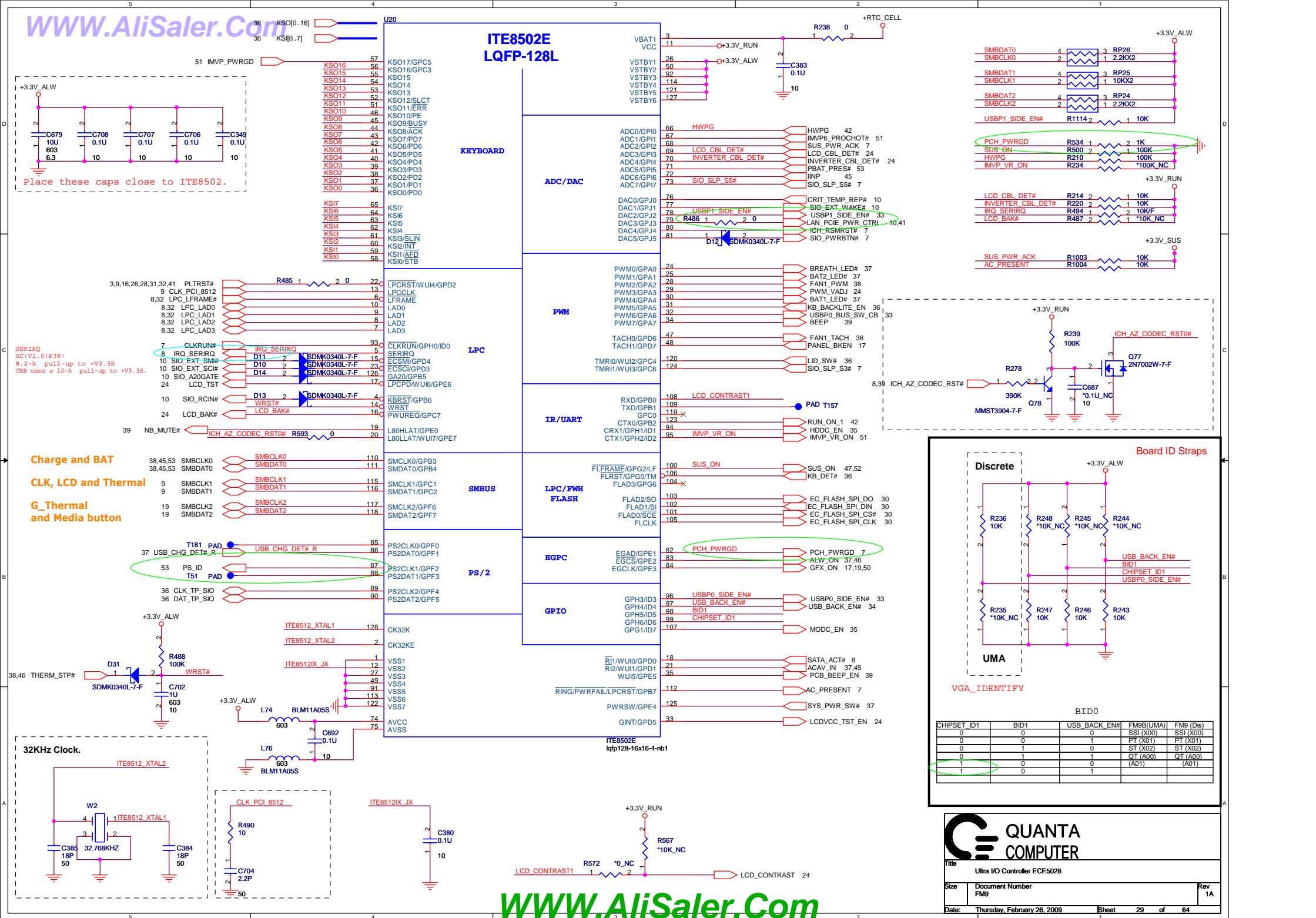
Express Card/CARD READER

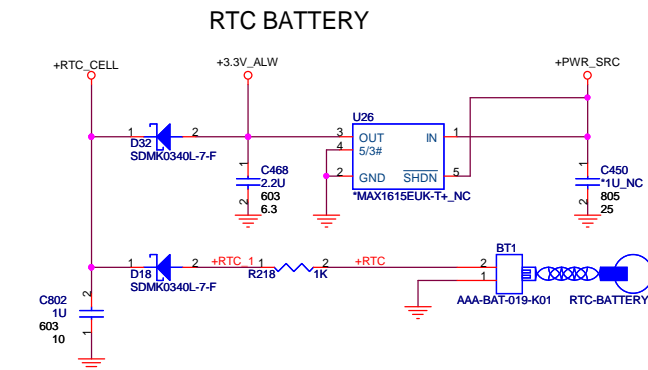
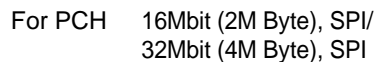


1394 CONNECTOR

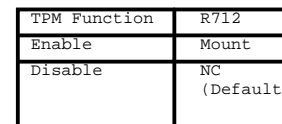
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

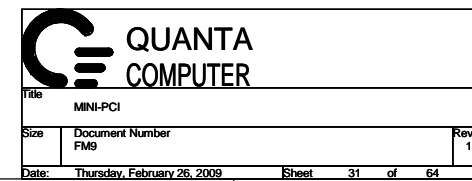
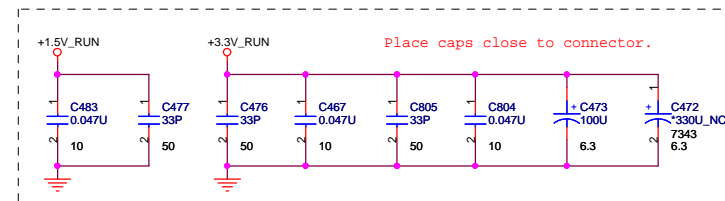




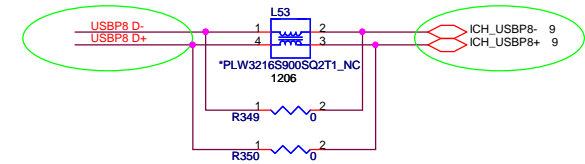
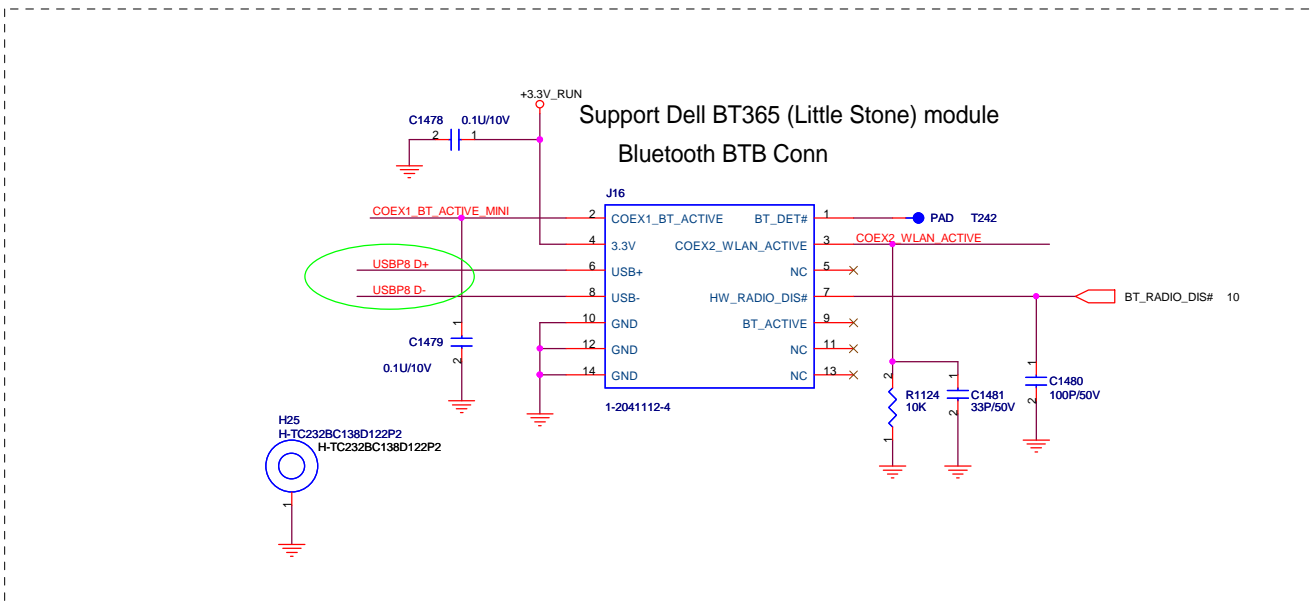
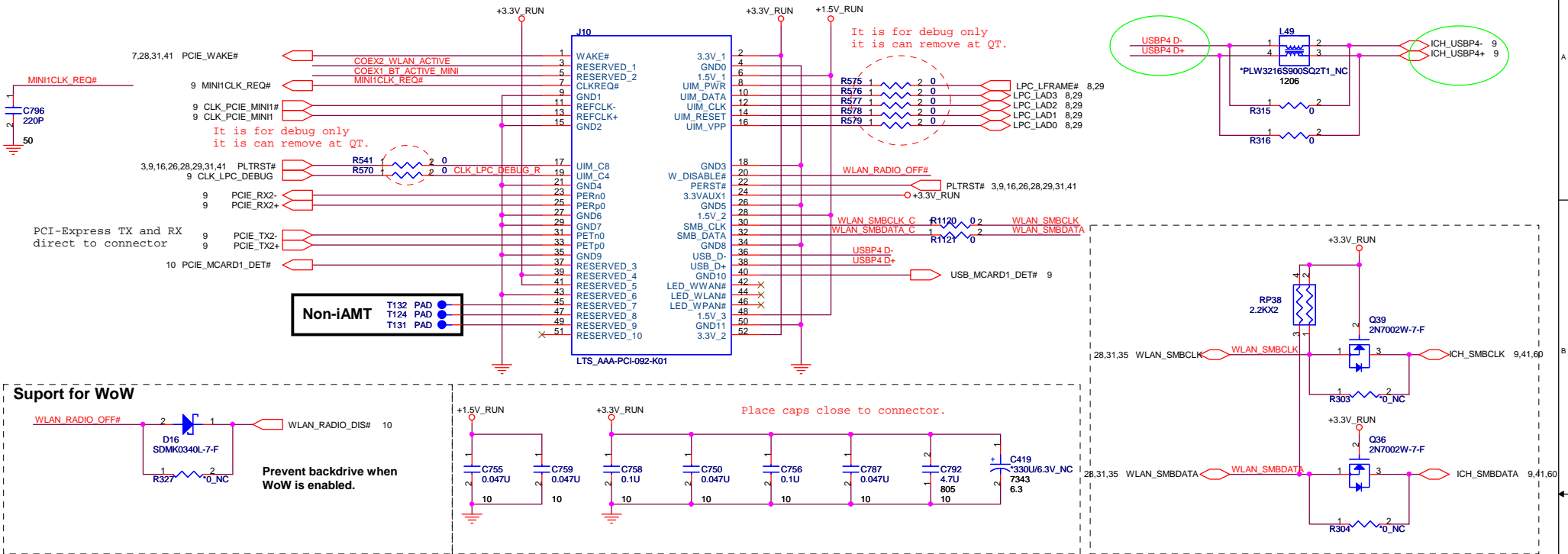


iTPM ENABLE/DISABLE

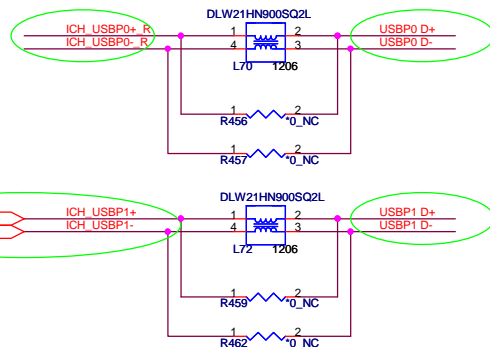




MiniCard WLAN connector

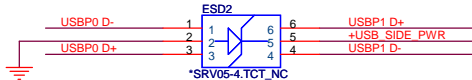


External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



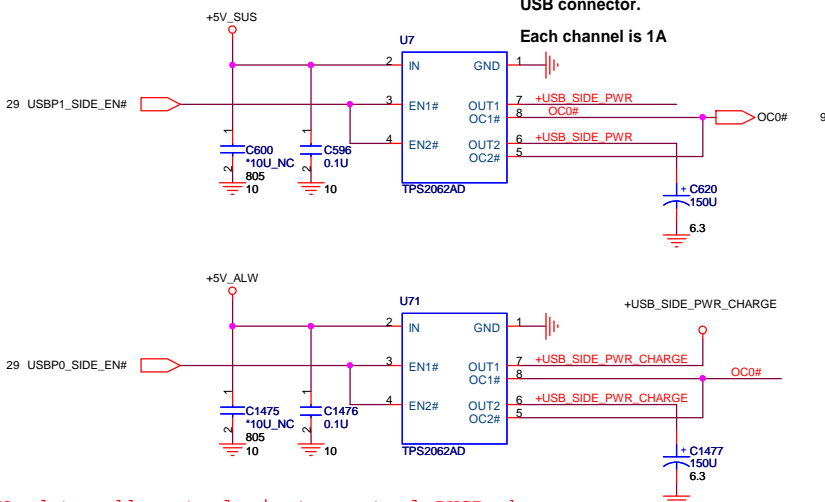
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

Each channel is 1A

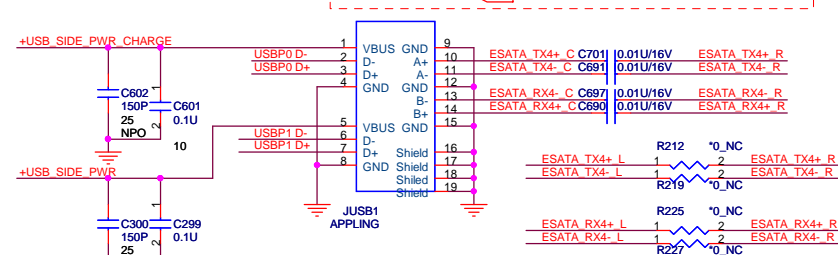


Need to add control pin to control PUSB charge

Support USBP1 charge function.
JUSB1 need to add USB_CHG_DET# pin wire to EC GPIO to detect USB device.

Side External USBX2

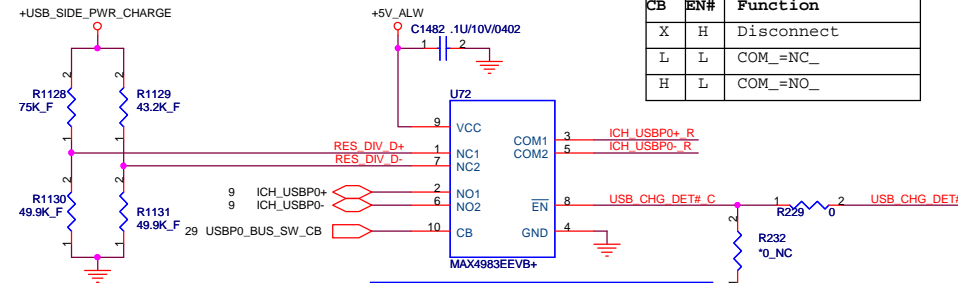
For USPI USB PWR CHARGE, JUSB1 need add USB_CHG_DET#



Please put those on the same side of MB PCB

USBx2 & ESATA COMBO & PWR CHARGE

USB BUS SW



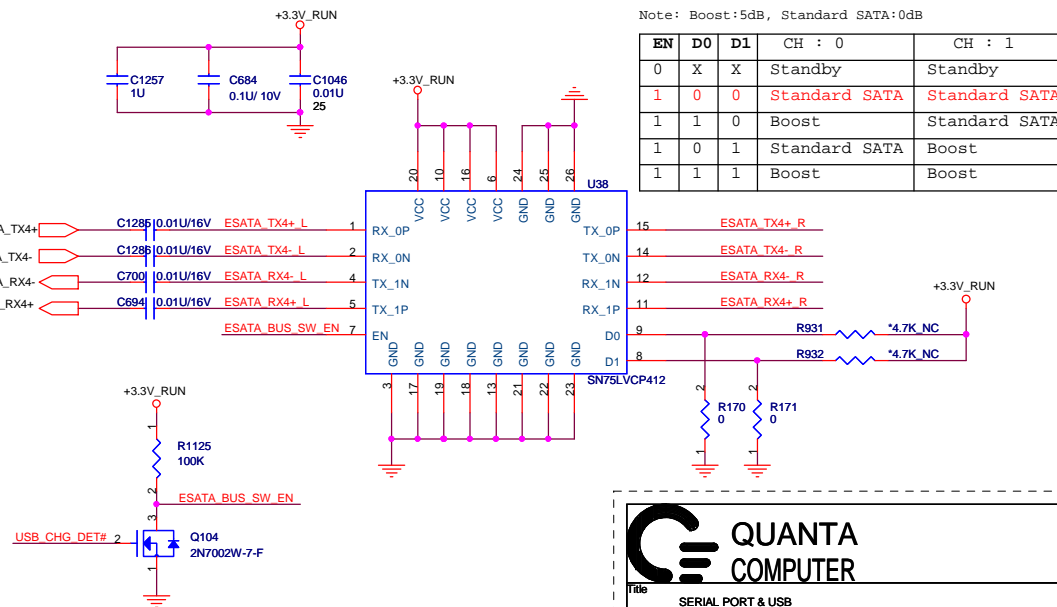
(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

CB	EN#	Function
X	H	Disconnect
L	L	COM_=NC_
H	L	COM_=NO_

E-SATA Re-driver

Please put those on the same side of MB PCB

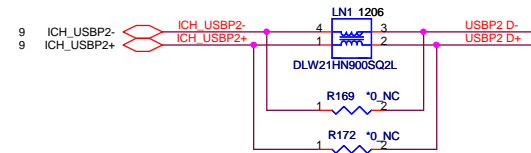
Note: Boost:5dB, Standard SATA:0dB



EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

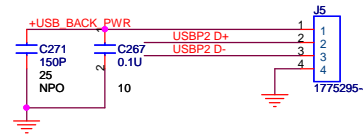
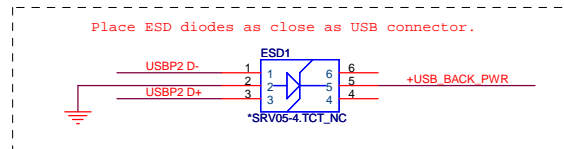
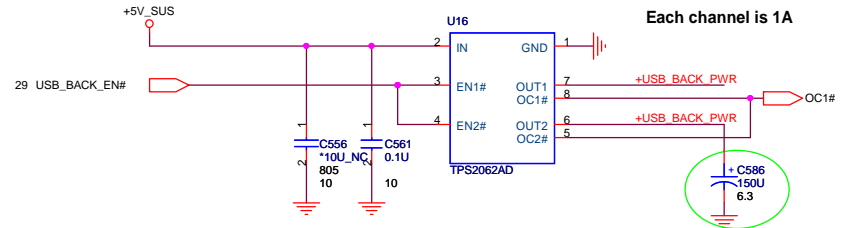
QUANTA
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Title SERIAL PORT & USB		
Size FMS	Document Number FMS	Rev 1A
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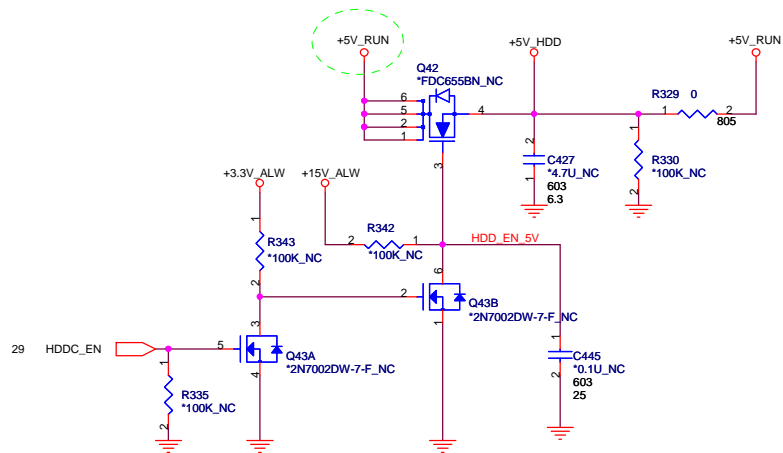
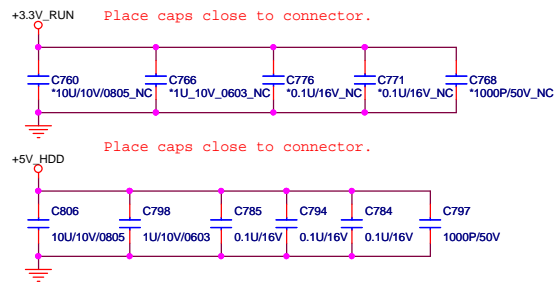
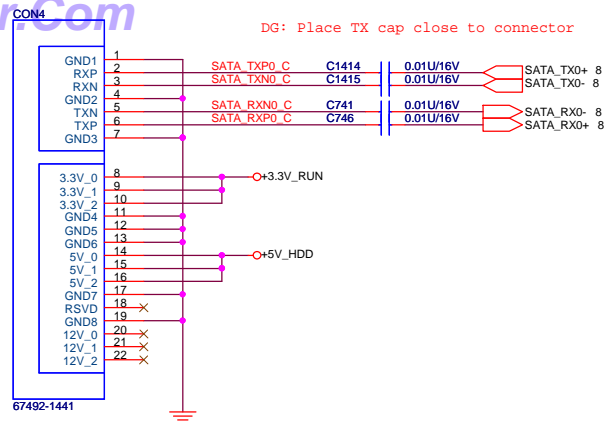


Place one 150uF cap by each USB connector.

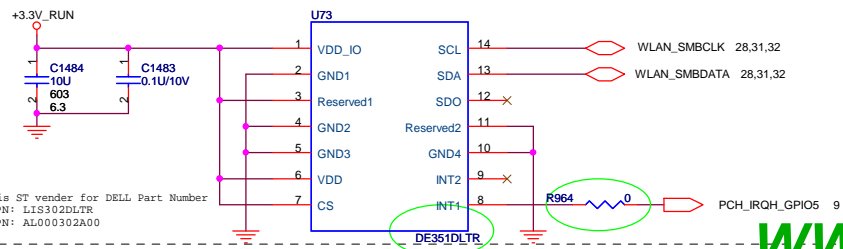
Each channel is 1A



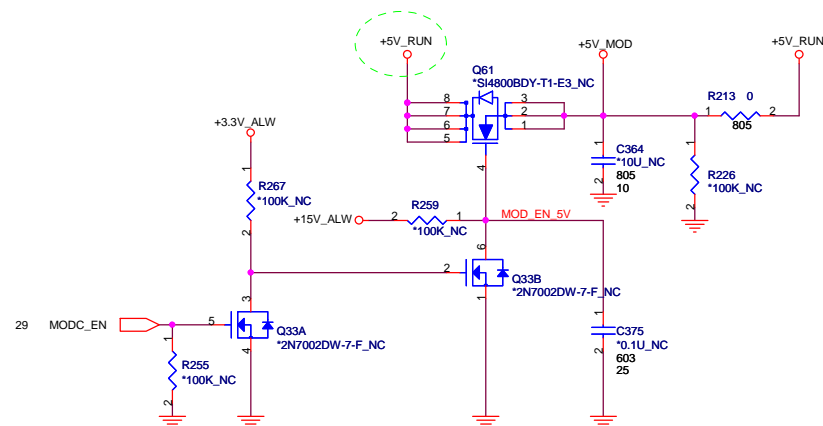
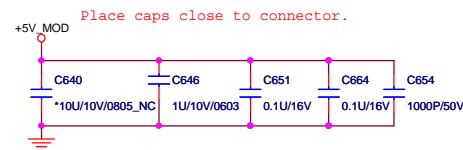
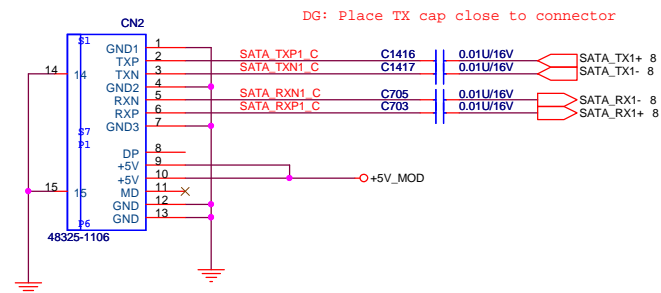
SATA Connector.



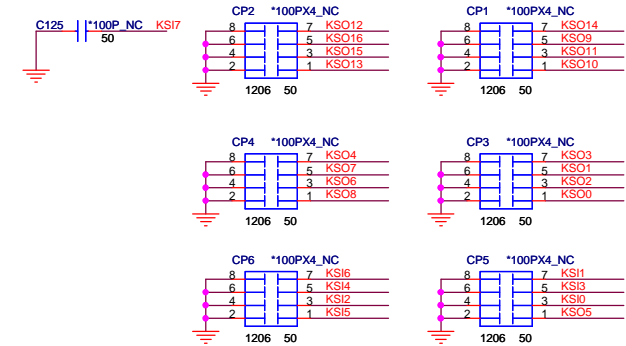
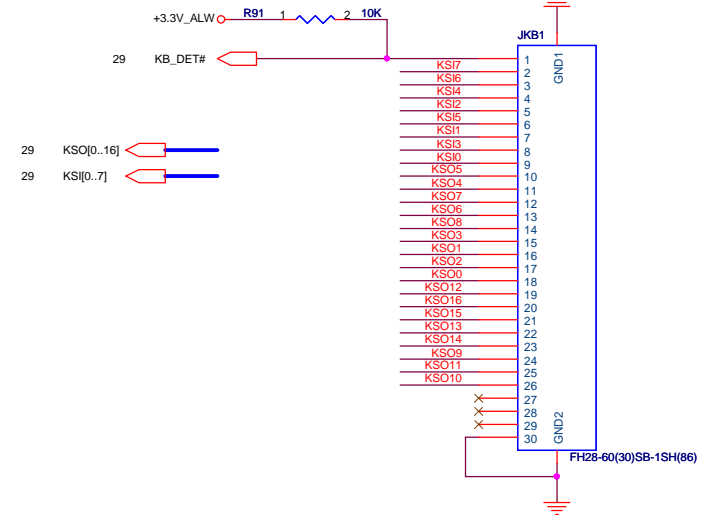
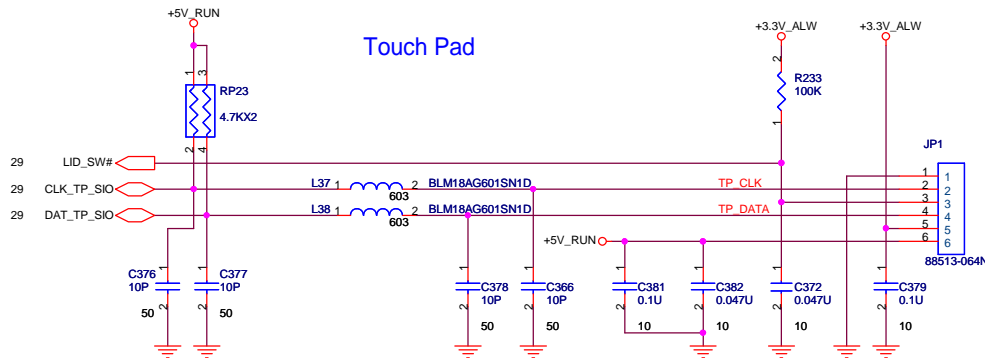
3-axis Fall Sensor (HDD data protector)



ODD Connector

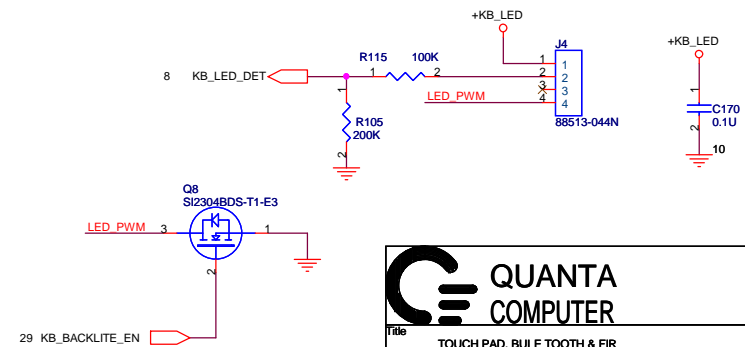
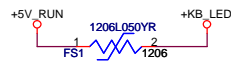


Title			SATA (HDD&CD_ROM)
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Key board illumination

+KB_LED power trace width >10 mil



QUANTA COMPUTER

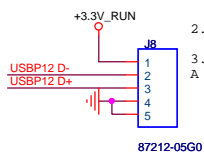
Title: TOUCH PAD, BULE TOOTH & FIR

Size: Document Number FM9 Rev 1A

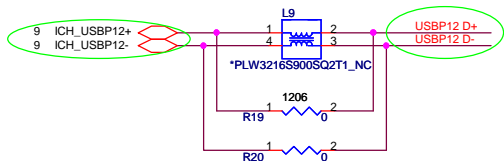
Date: Thursday, February 26, 2009 Sheet 36 of 64

Touch Screen Module

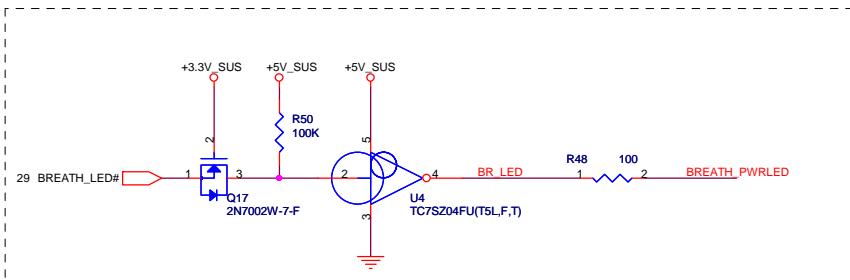
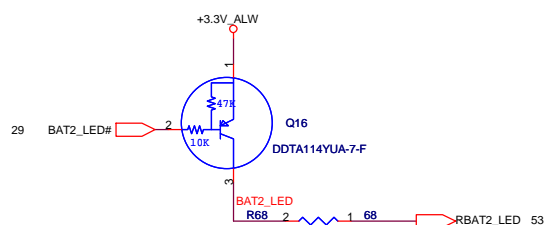
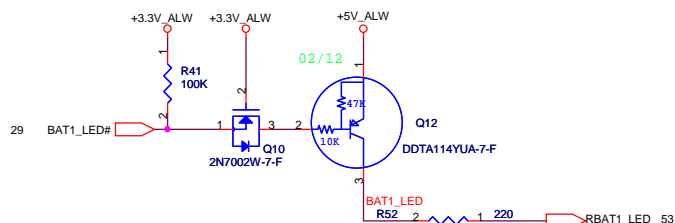
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 2. Maximum cable resistance on VCC, GND should be 150m ohm.
 3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



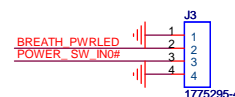
Need check the connector footprint and symbol.



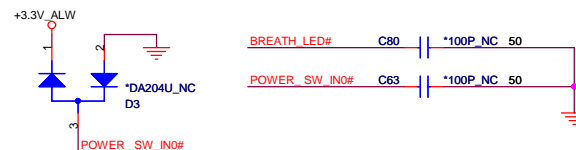
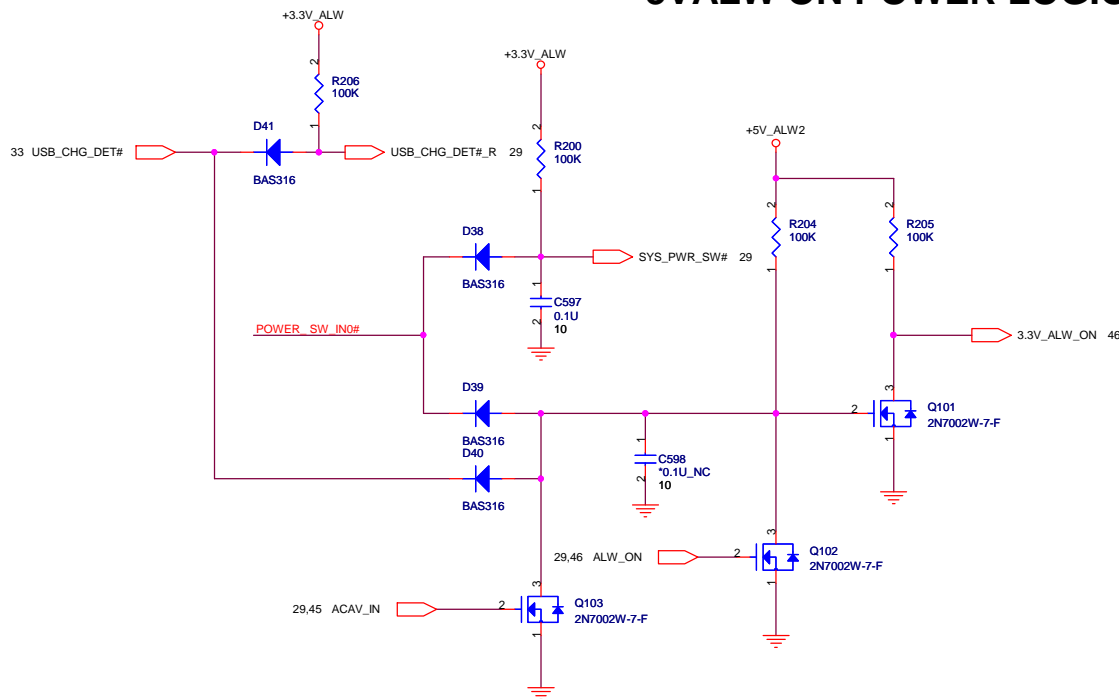
Battery status.



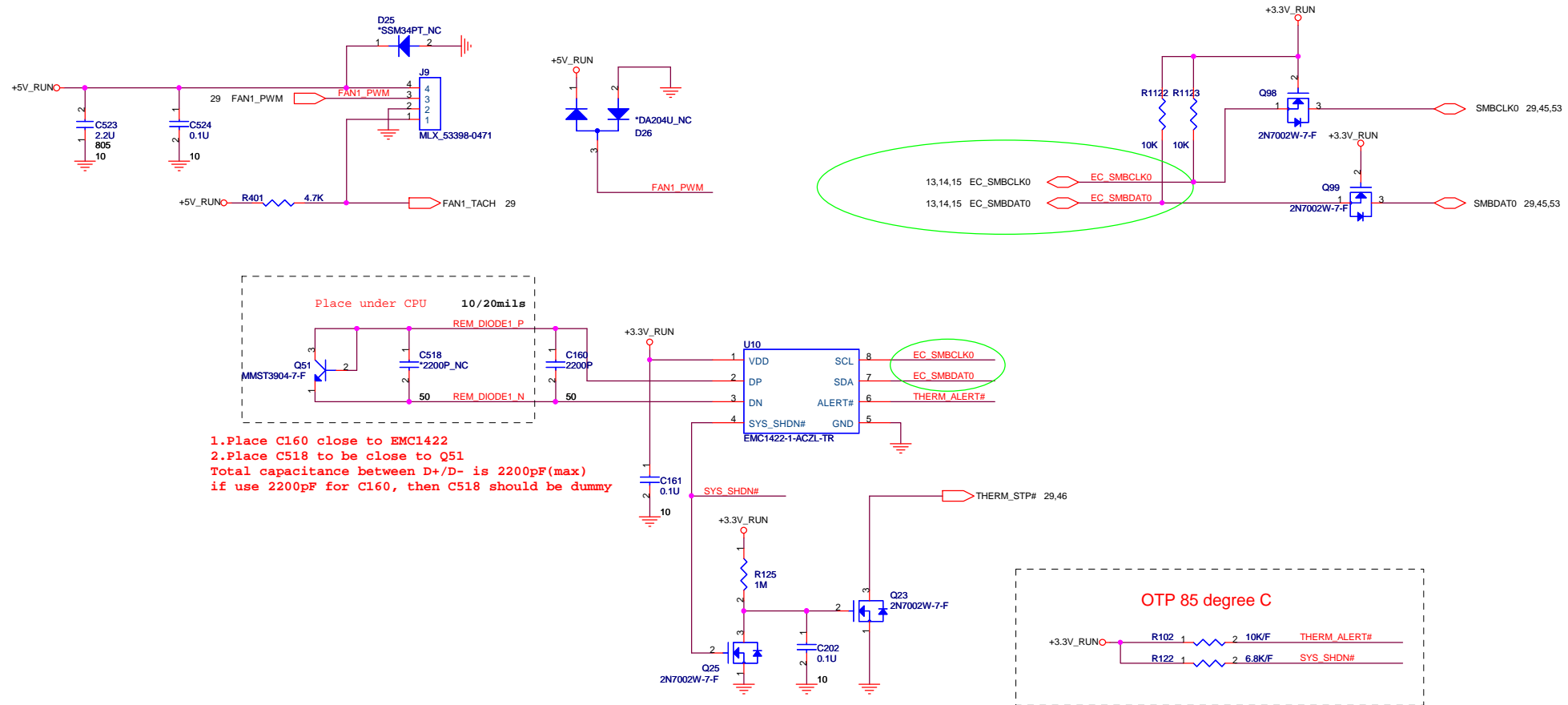
Power button Cable

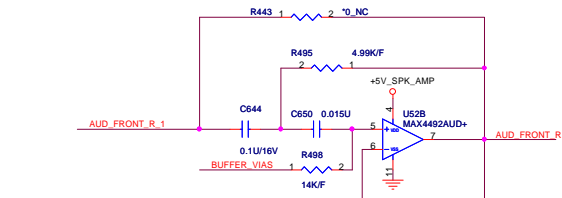
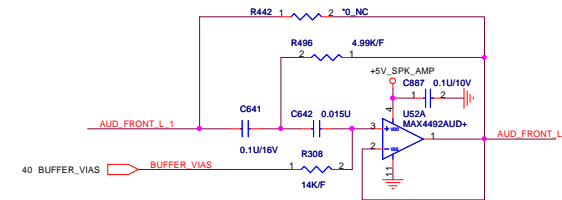


3VALW ON POWER LOGIC

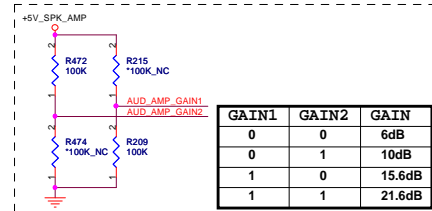
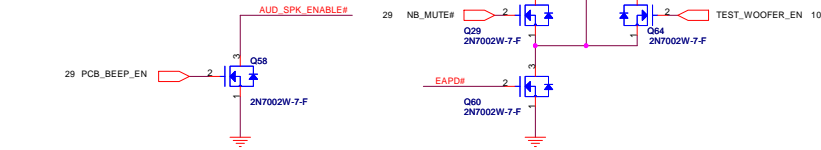


Title		
SWITCH, KEYBOARD & LED&Touch Screen Module		
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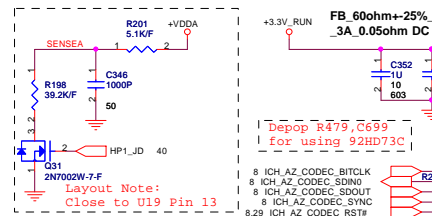
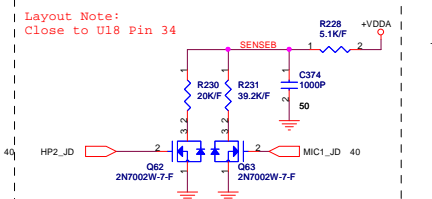
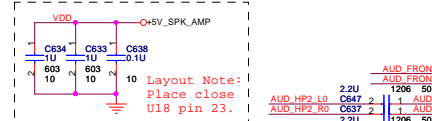




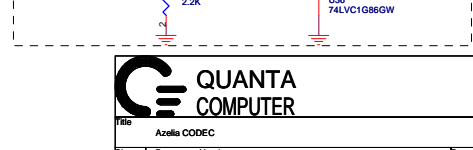
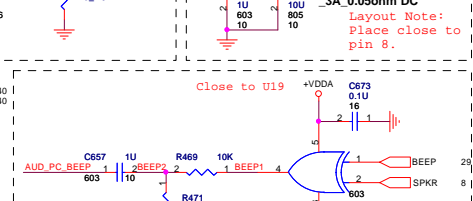
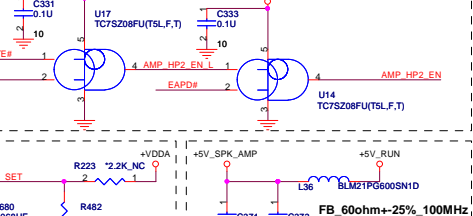
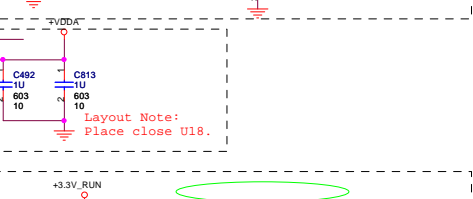
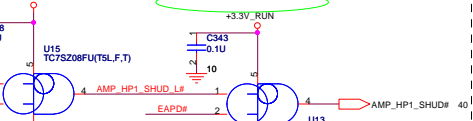
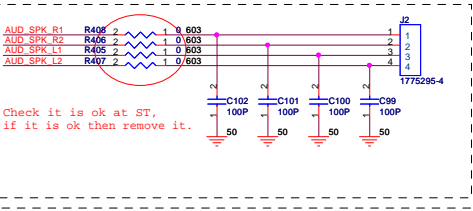
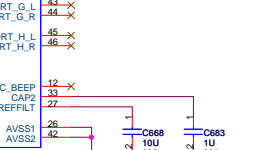
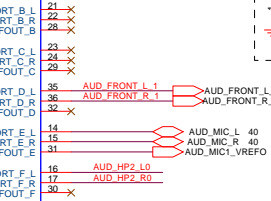
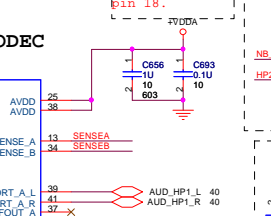
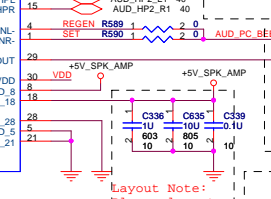
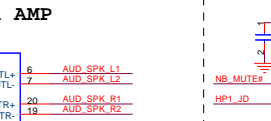
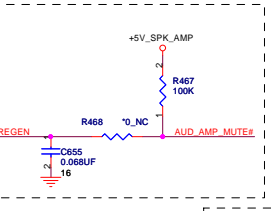
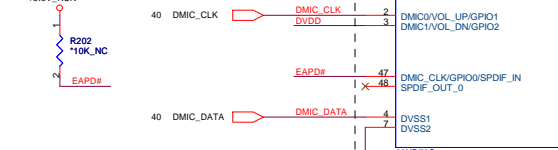
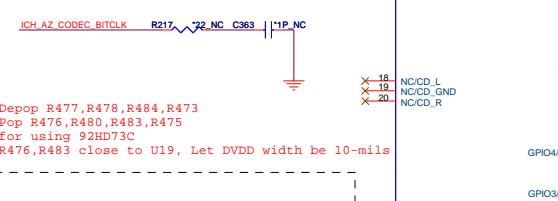
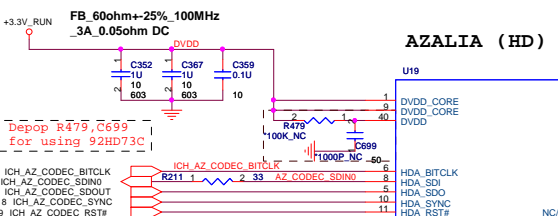
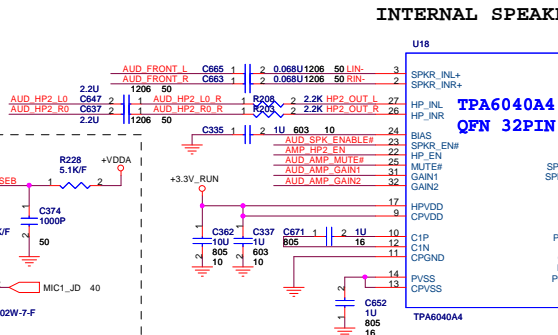
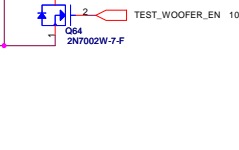
EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK_ENABLE#	WOOFER_EN
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofers)
1	1	0	L (Test SPK)	L (Disable Woofers)
1	1	1	L	H



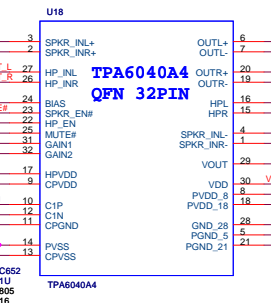
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



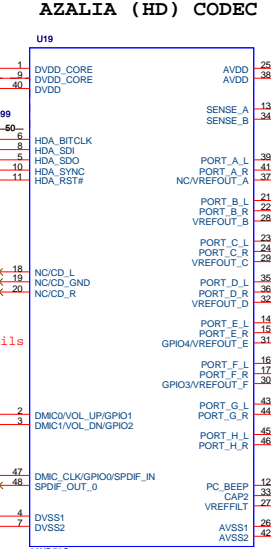
EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK_ENABLE#	WOOFER_EN
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofers)
1	1	0	L (Test SPK)	L (Disable Woofers)
1	1	1	L	H



INTERNAL SPEAKER AMP



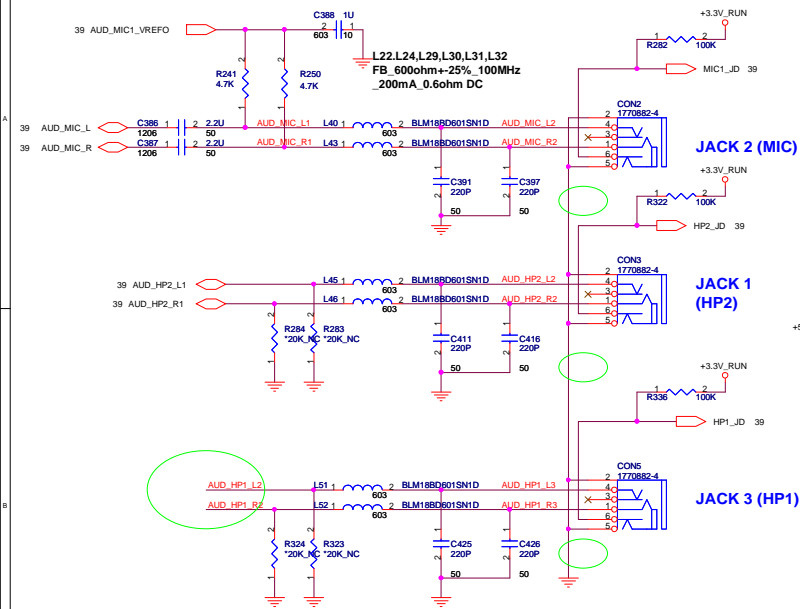
AZALIA (HD) CODEC



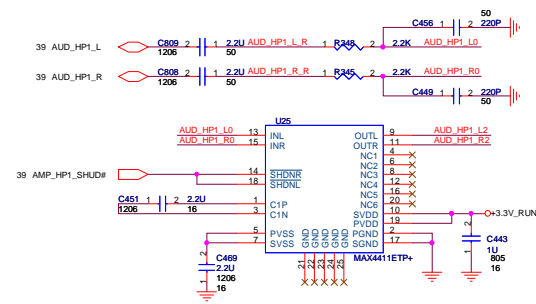
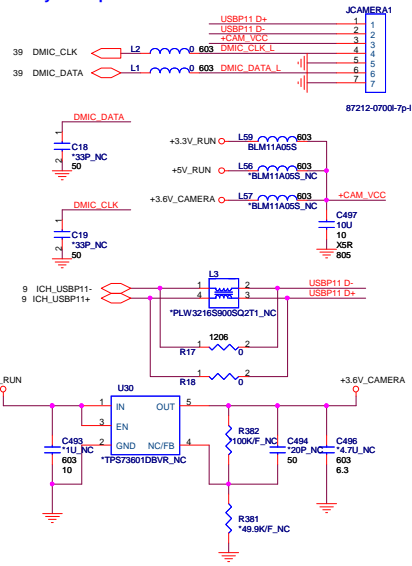
QUANTA COMPUTER

File	Azalia CODEC	Rev	1A
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	FMB		
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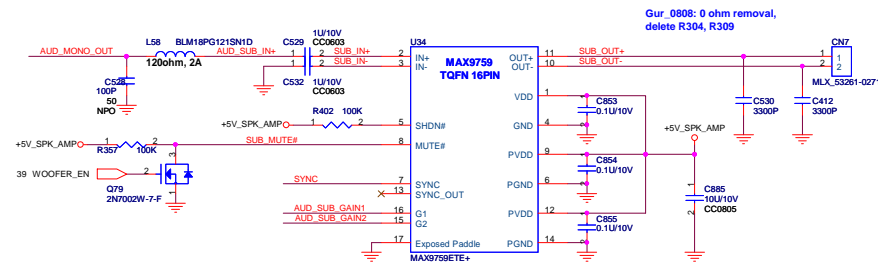
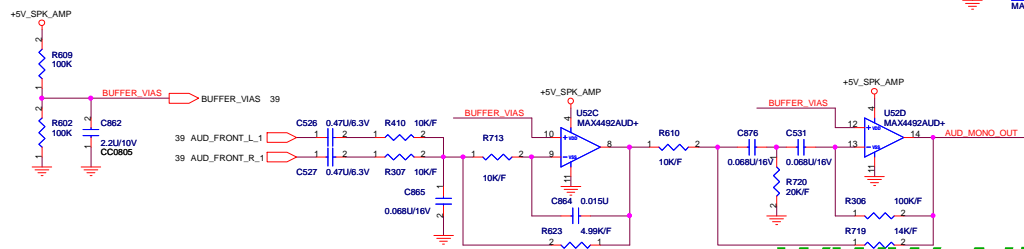
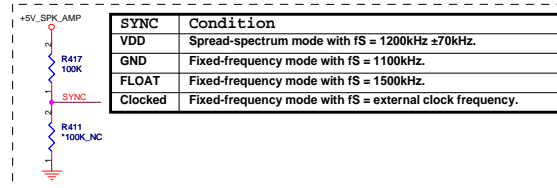
Headphone Jack
Stereo MIC Jack



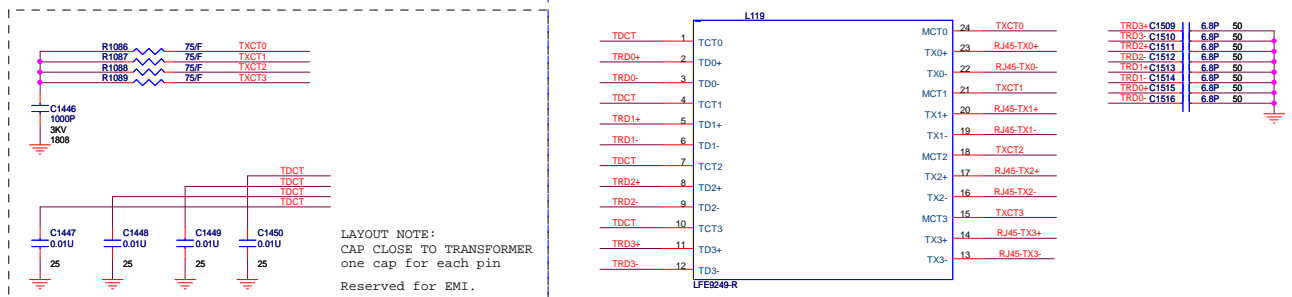
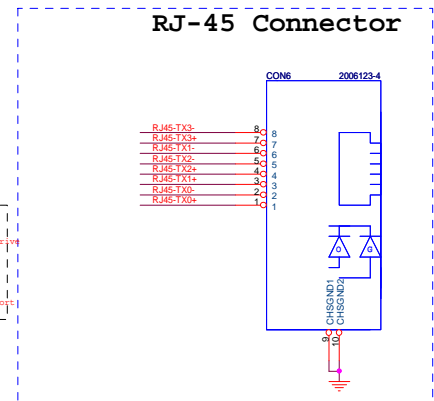
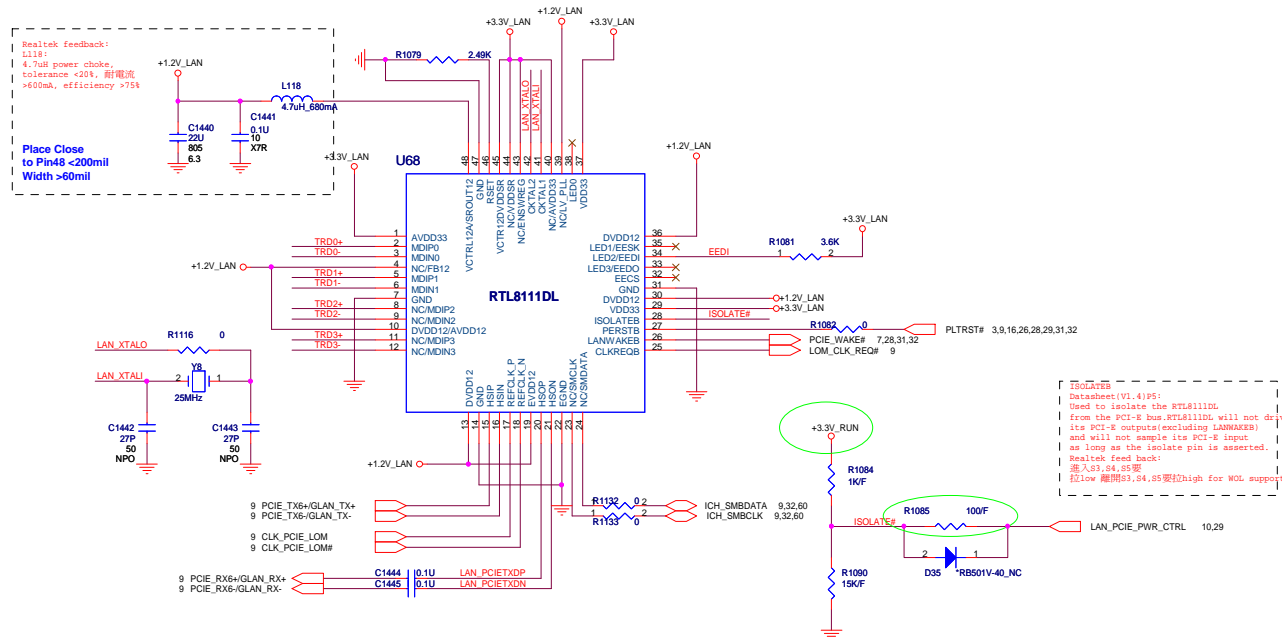
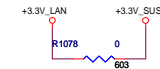
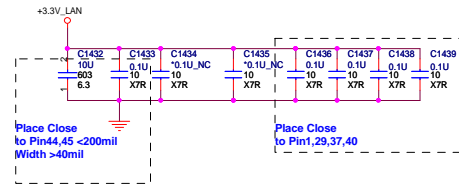
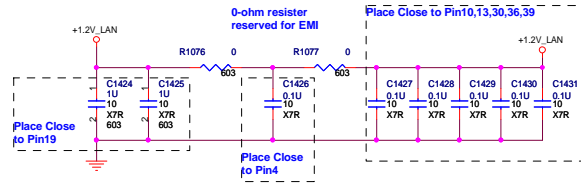
Array Microphone & Camera

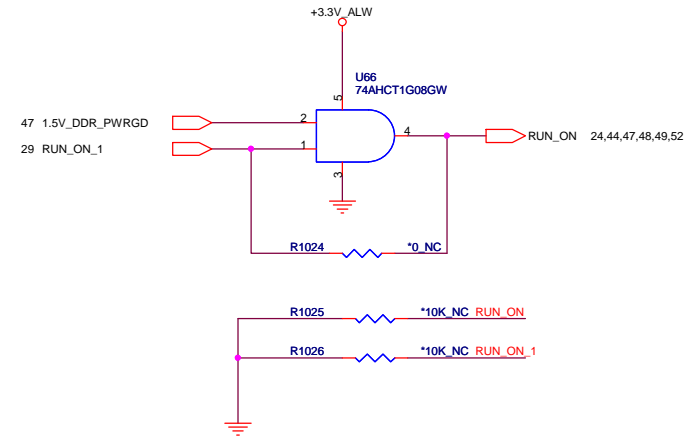
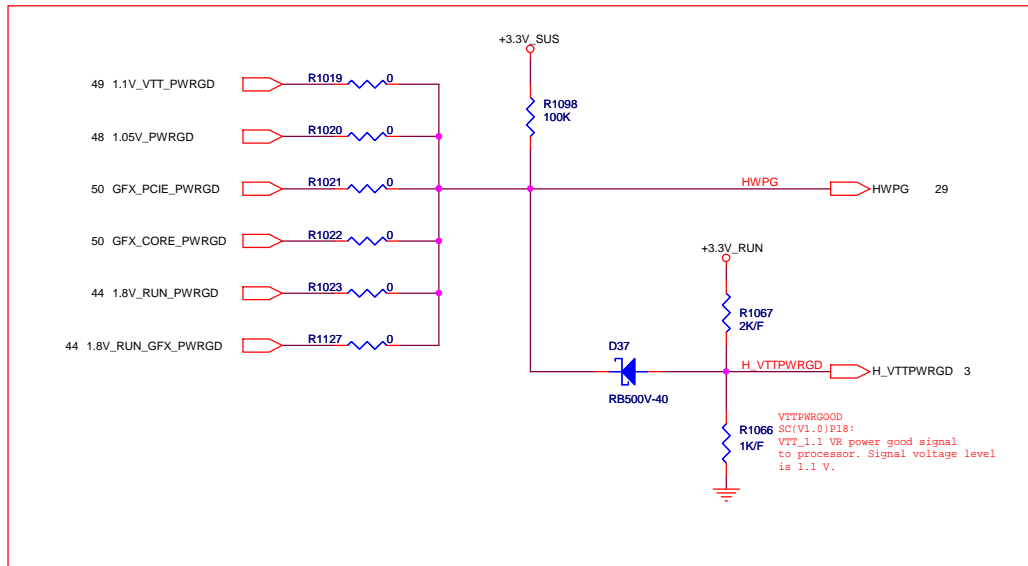
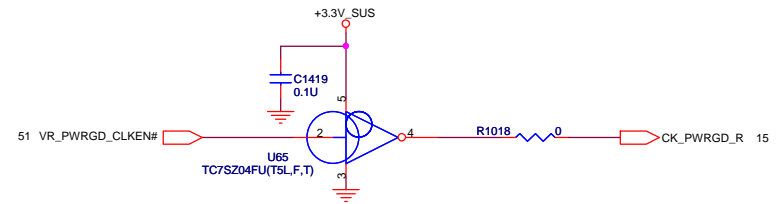
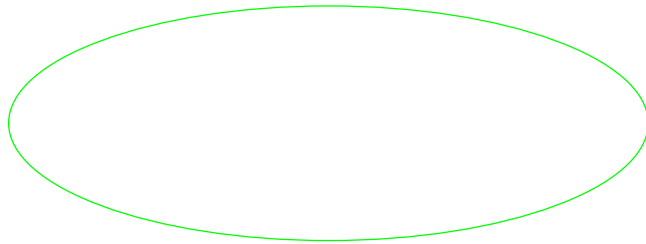



INTERNAL SUBWOOFER AMP

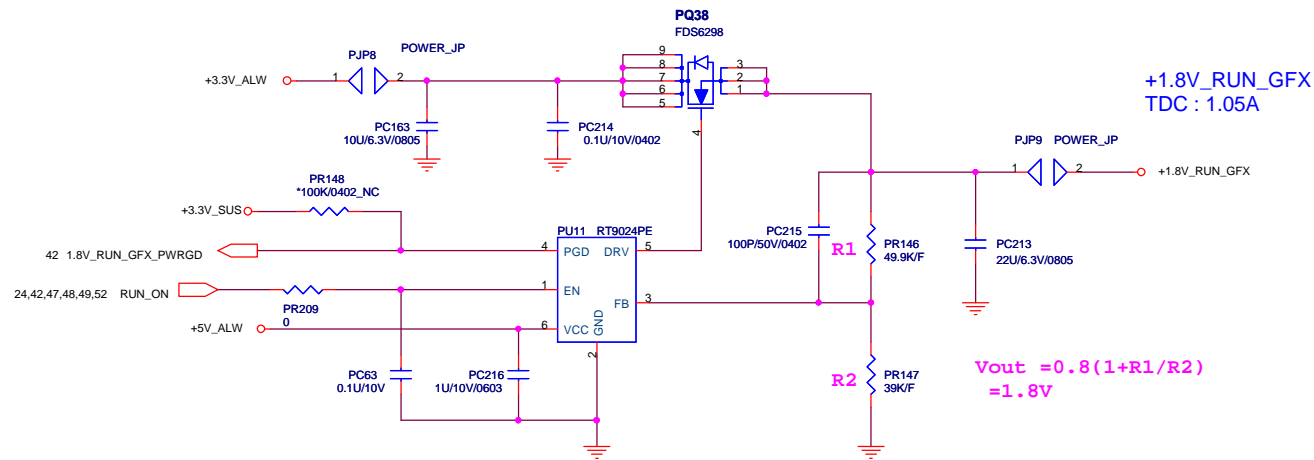


GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

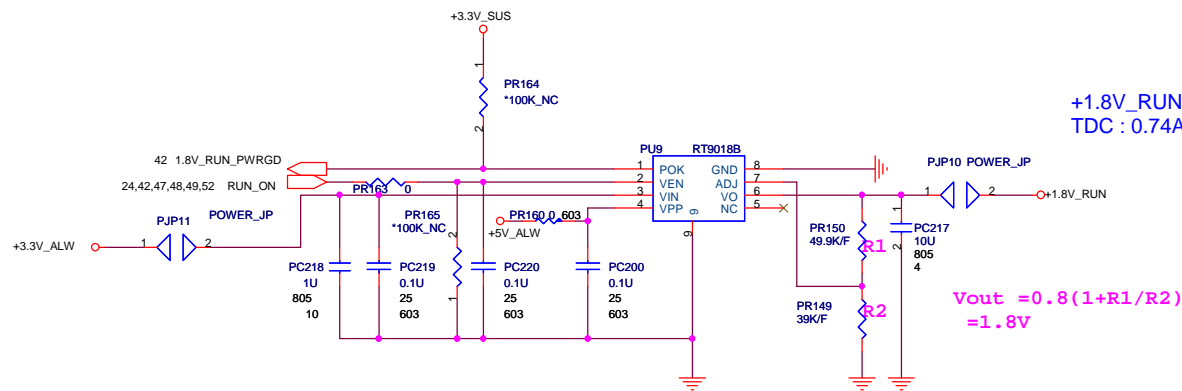




 QUANTA COMPUTER		
Title Battery Selector		
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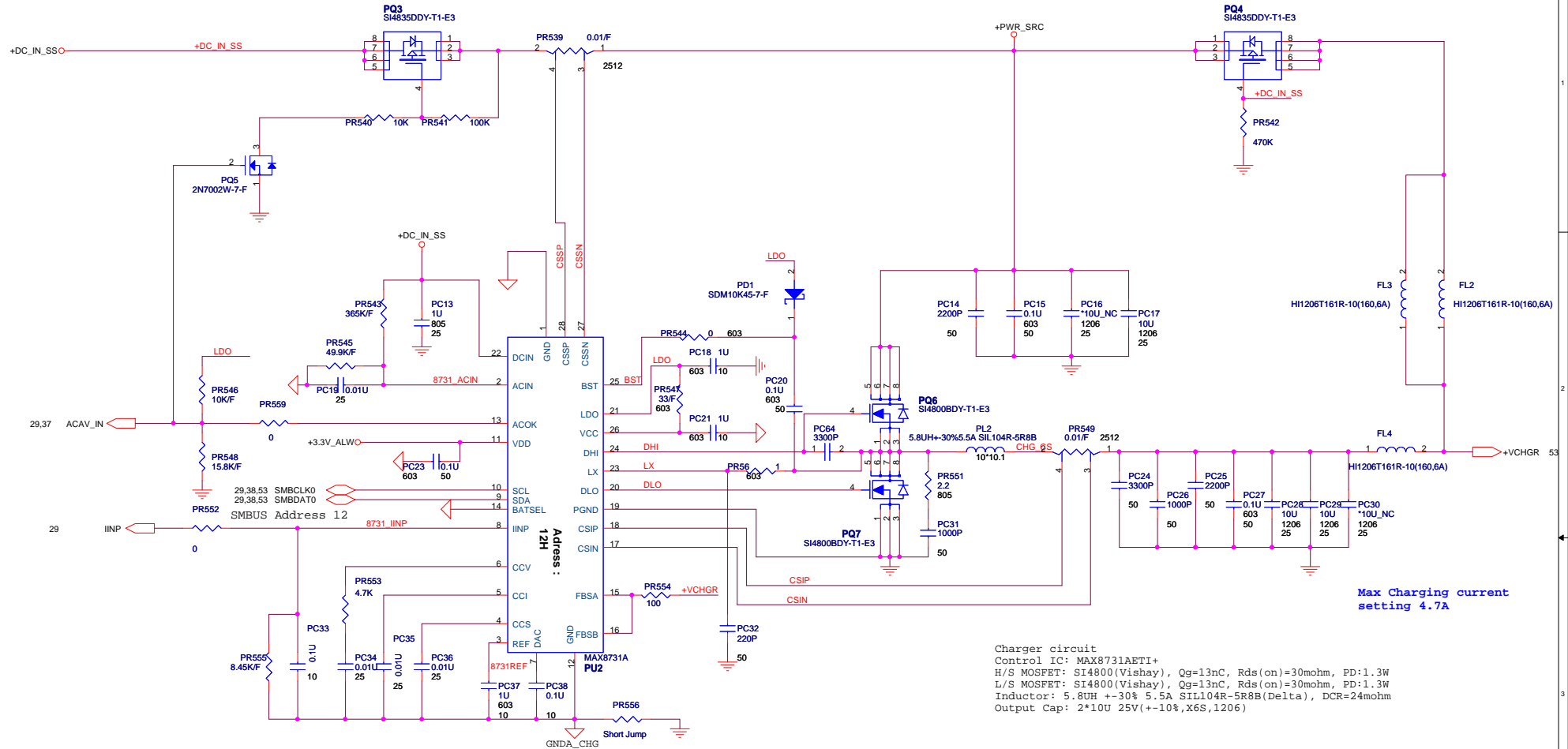
+1.8V_RUN_GFX for VGA 1.8V
+1.8V_RUN for CPU and PCH 1.8V



Title		
+1.8V_RUN_GFX (RT9024PE) & +1.8V_RUN(RT9018B)		
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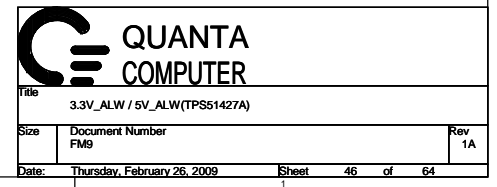
Continuous current : 13A
Rds(on) : 18mohm

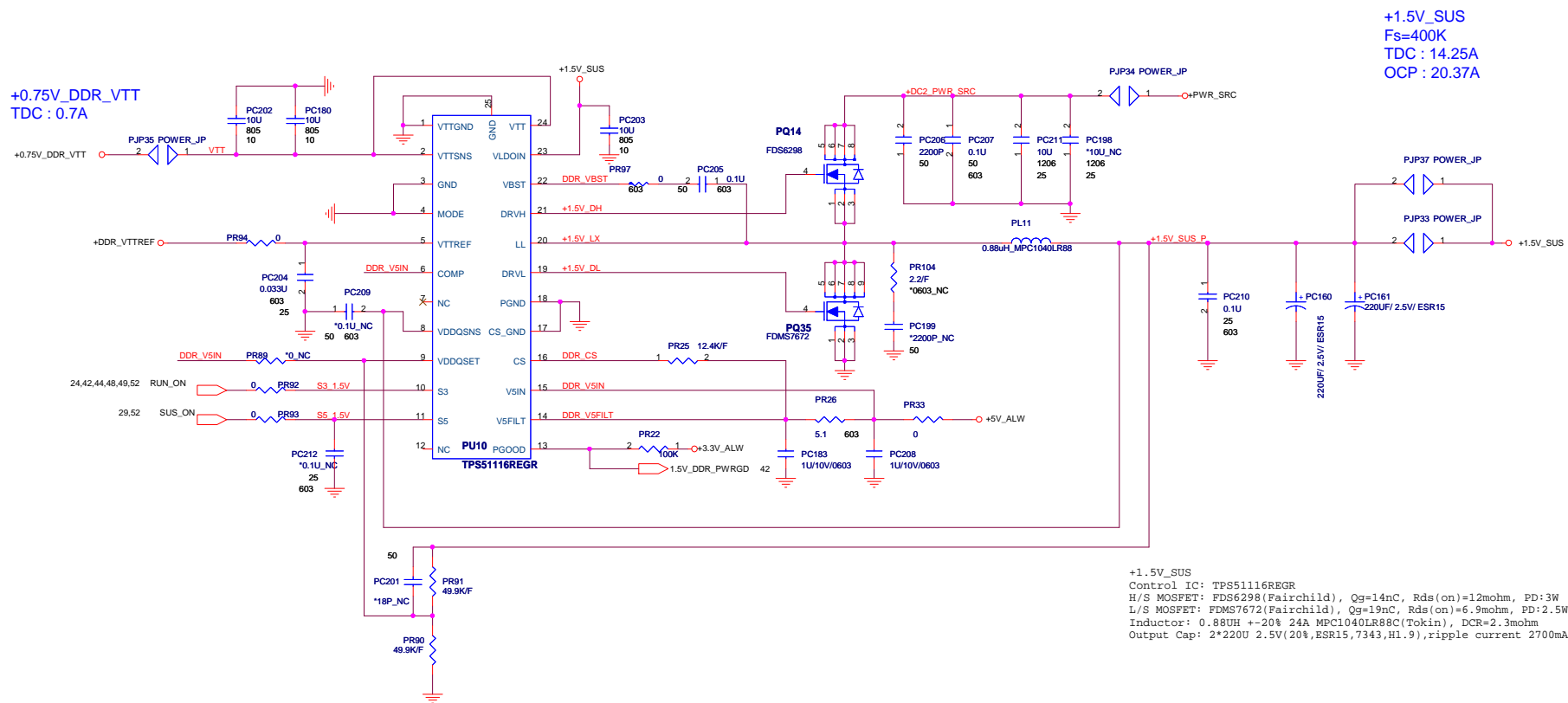
Continuous current : 13A
Rds(on) : 18mohm



QUANTA
COMPUTER

Title			Charger (MAX8731)
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VDDQ and VTT discharge control

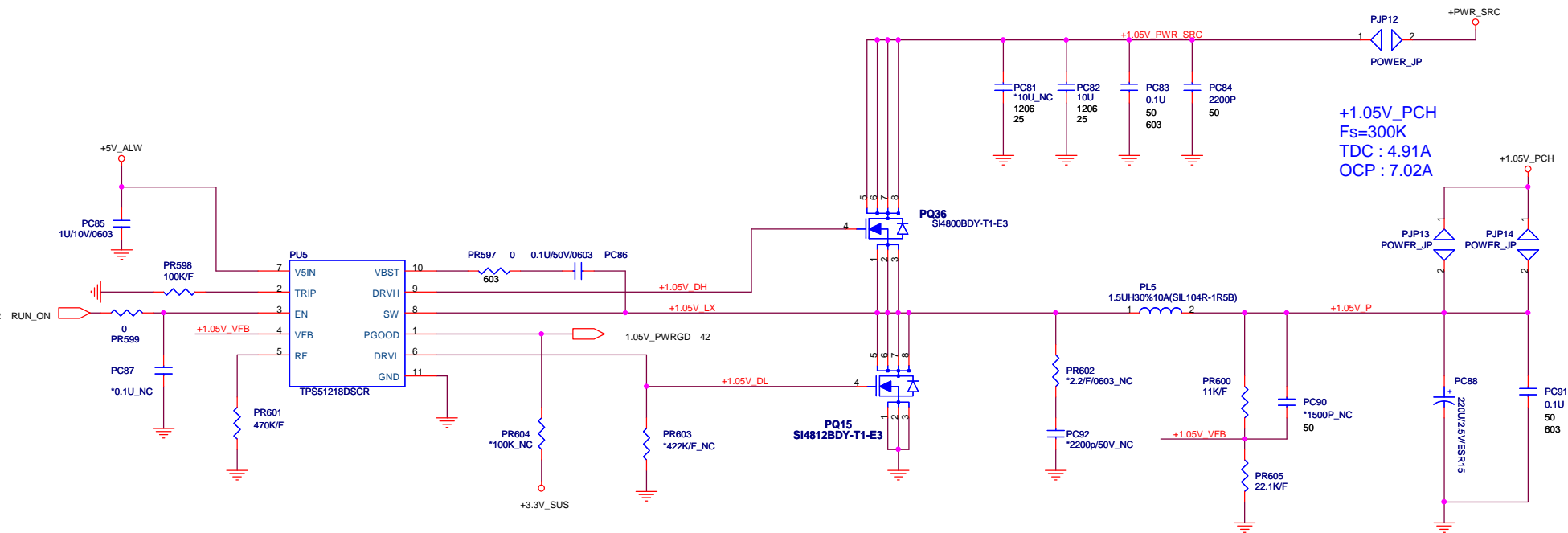
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

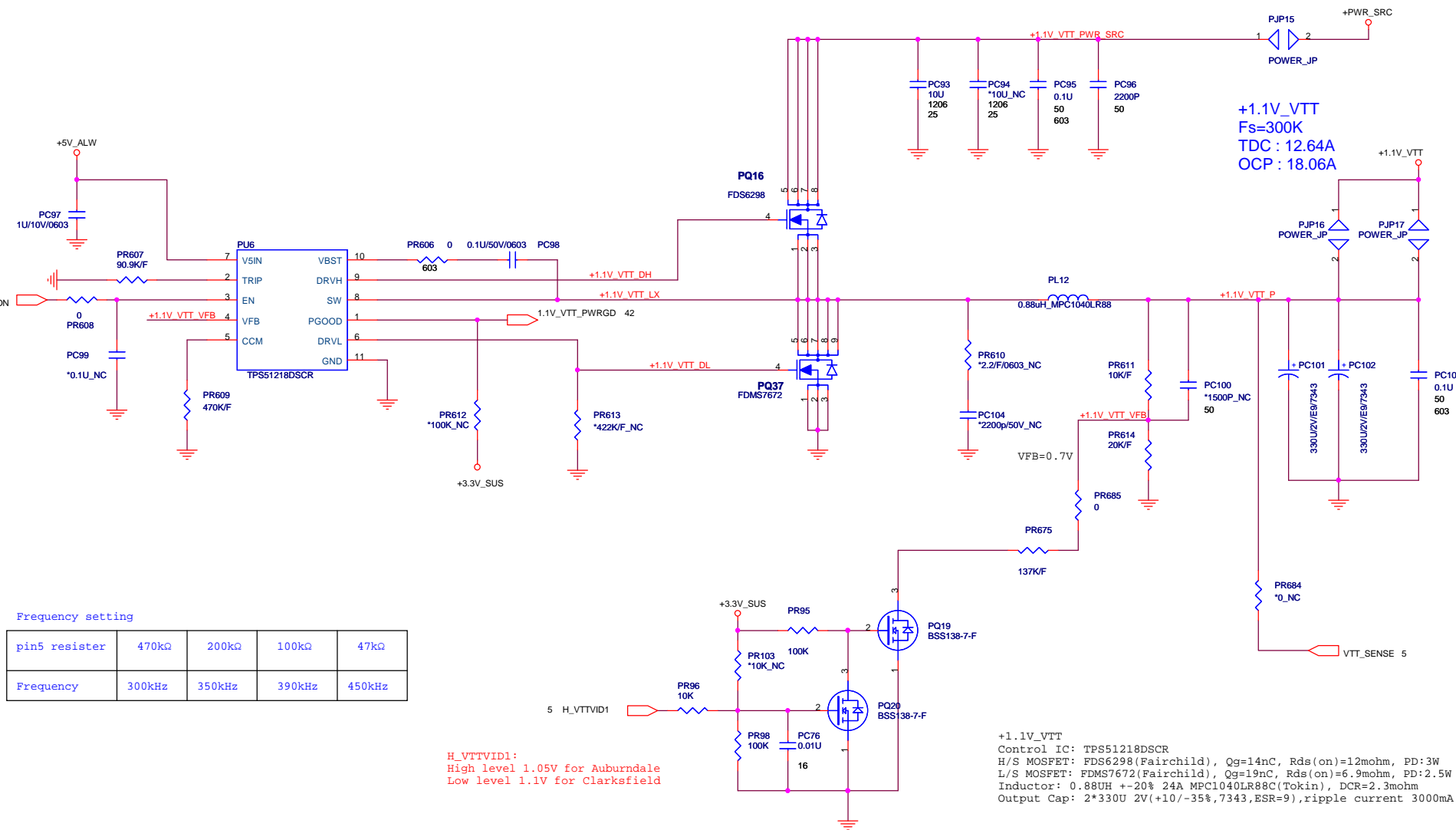
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



+1.05V_PCH
Fs=300K
TDC : 4.91A
OCP : 7.02A

```
+1.05V_PCH
Control IC: TPS51218DSCR
H/S MOSFET: SI4800BYD-T1-E3(Vishay), Qg=13nC, Rds(on)=30mohm, PD:1.3W
L/S MOSFET: SI4812BYD-T1-E3(Vishay), Qg=13nC, Rds(on)=21mohm, PD:1.4W
Inductor: 1.5uH + 25% 10A SIL104R-IR5B(Delta), DCR=8.1mohm
Output Cap: 1*220U + 30V(20%,ESR15,7343,H1.9),ripple current 2700mA
```

Frequency setting				
pin5 resistor	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

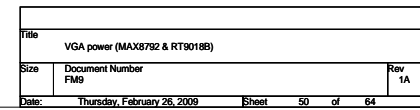


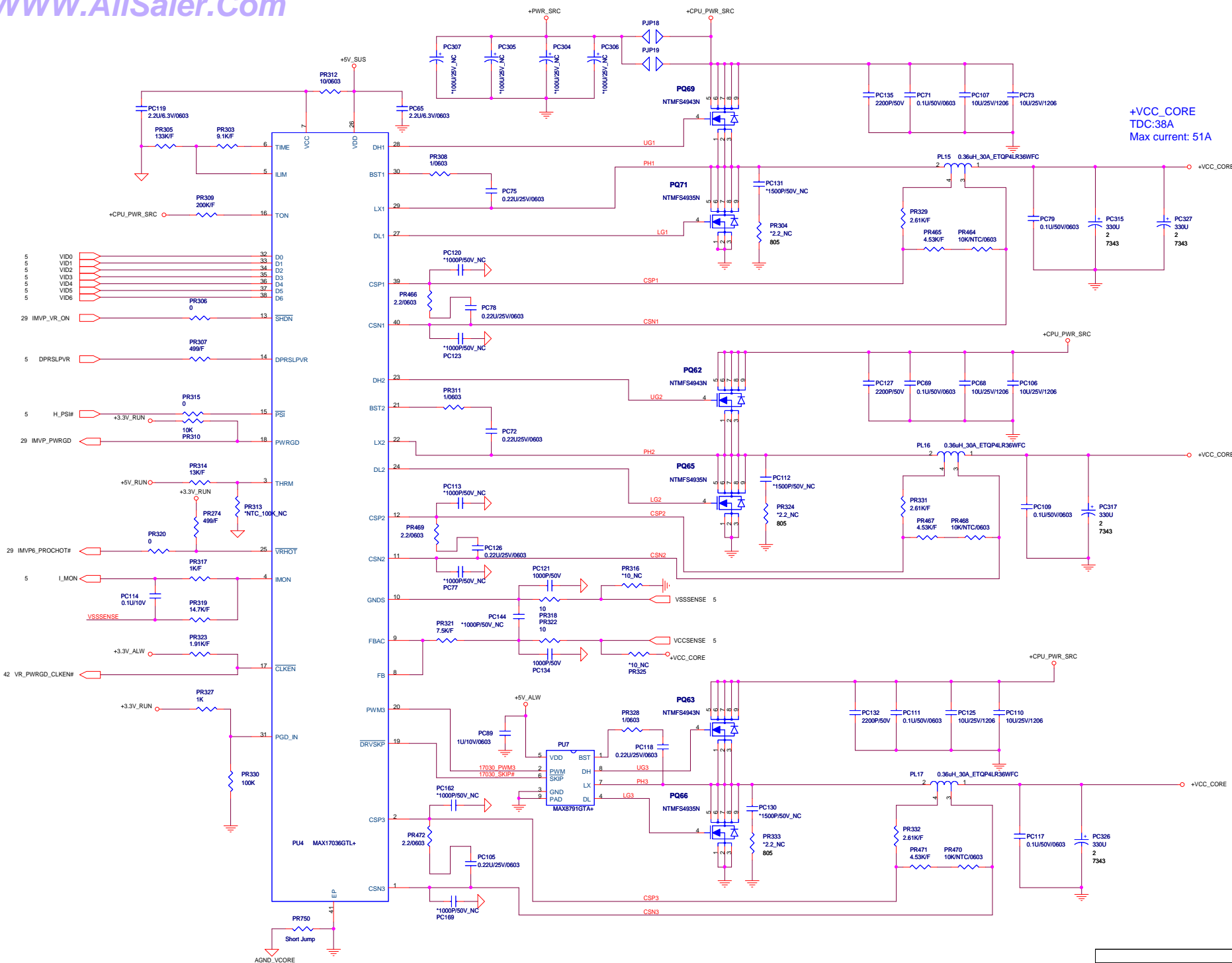
Frequency setting

pin5 resistor	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

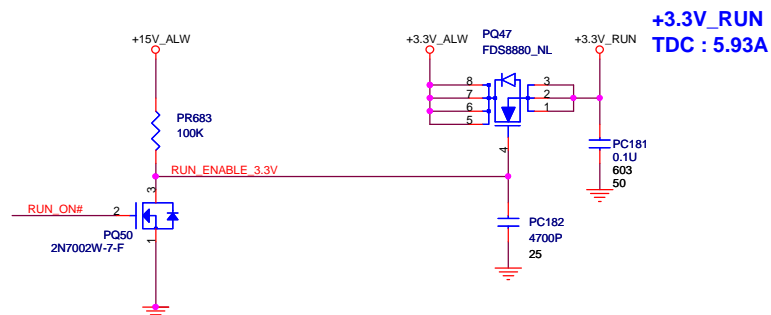
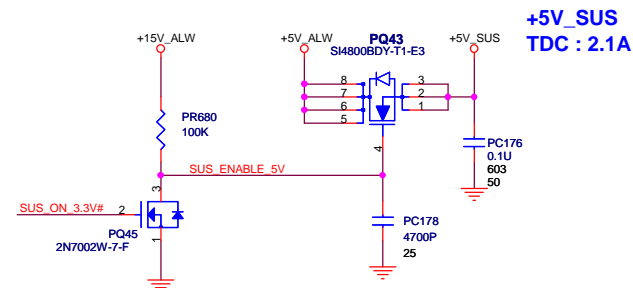
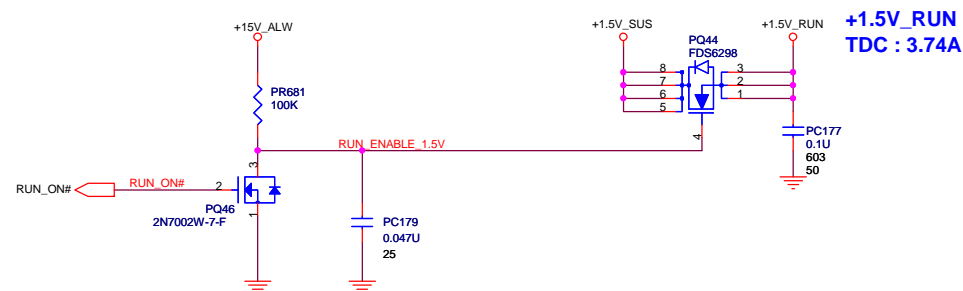
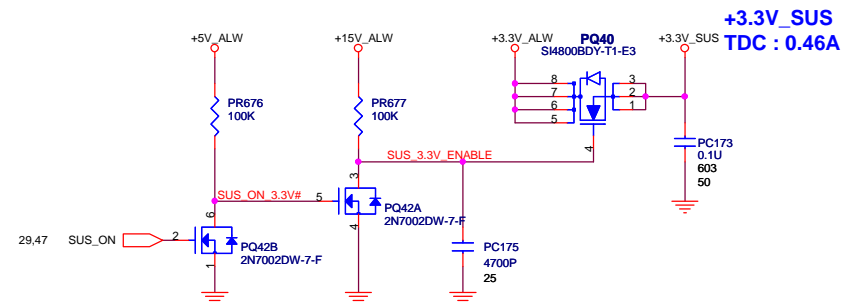
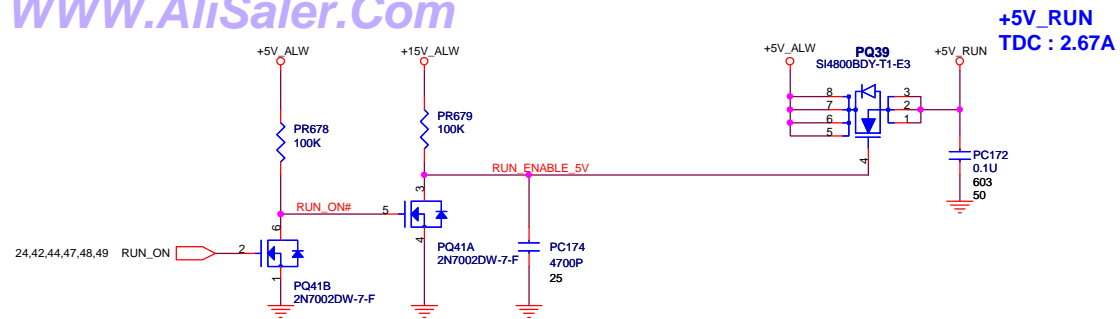
```
H_VTTVID1:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield
```

```
+1.1V_VTT
Control IC: TPS51218(DSCR
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDSM7672(Fairchild), Qg=19nC, Rds(on)=6.9mohm, PD:2.5W
Inductor: 0.88uH +20% 24A MPC1040LR88C(Tokin), DCR=2.3mohm
Output Cap: 2*330u 2V(+10/-35%,7343,ESR=9),ripple current 3000mA
```

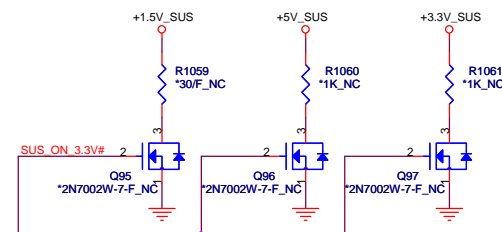
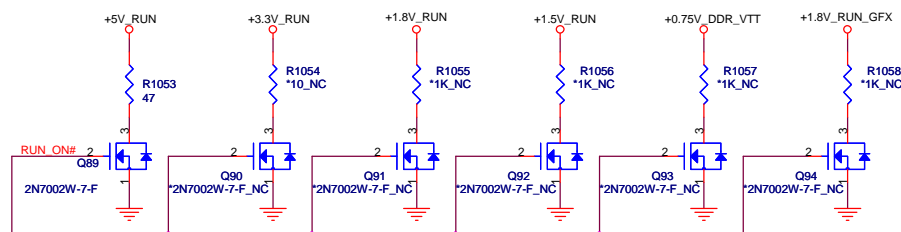




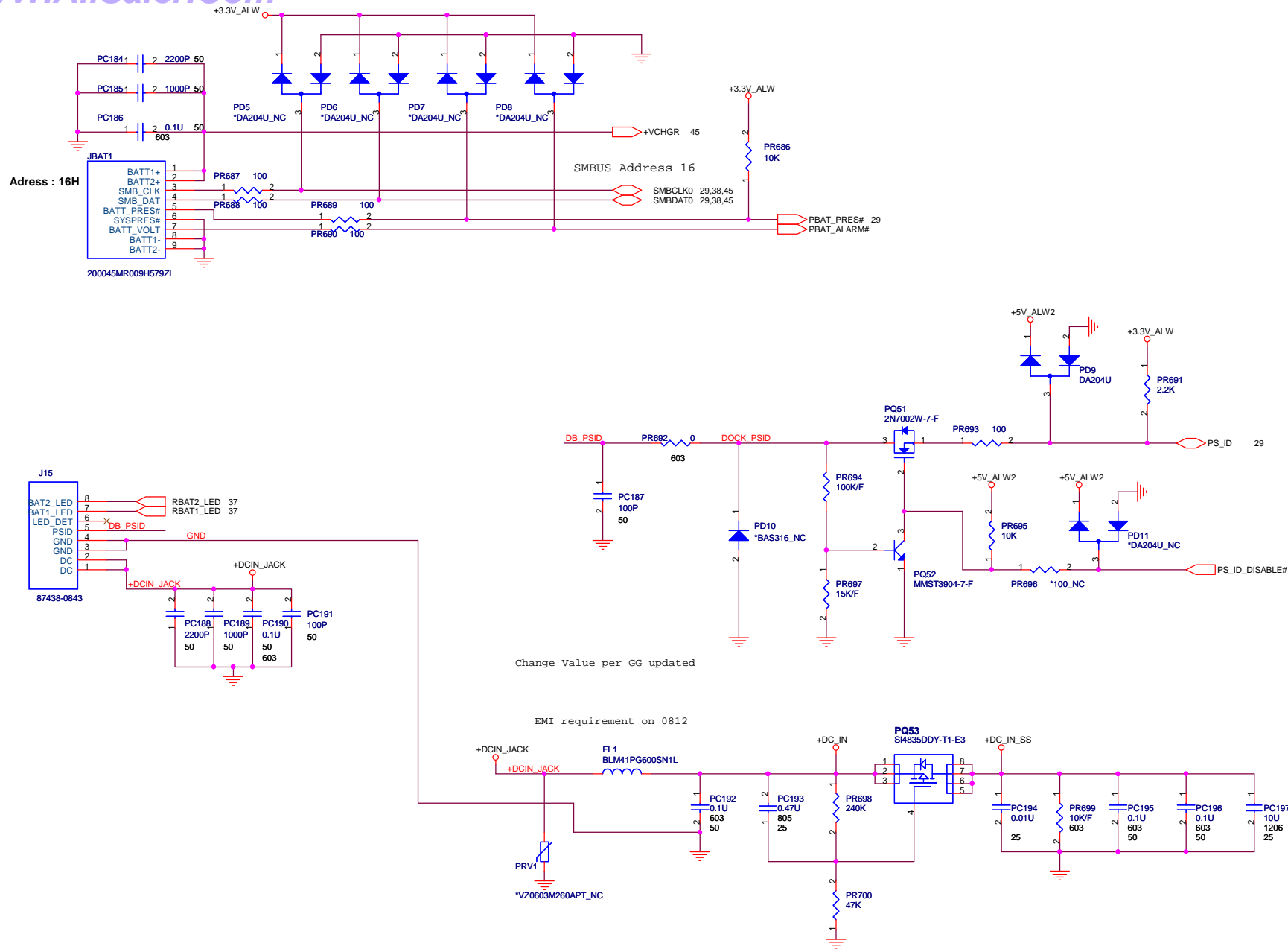
+VCC_CORE
TDC:38A
Max current: 51A



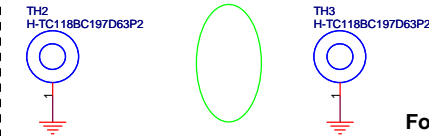
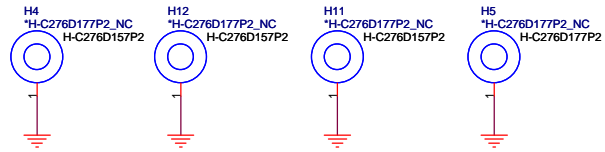
Reserve discharge path



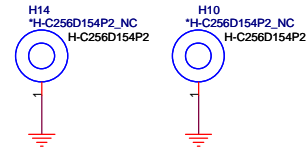
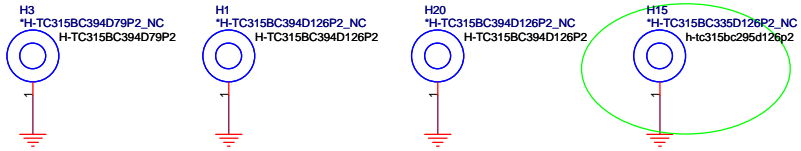
Title RUN / SUS POWER SW		
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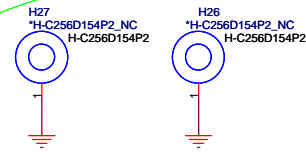
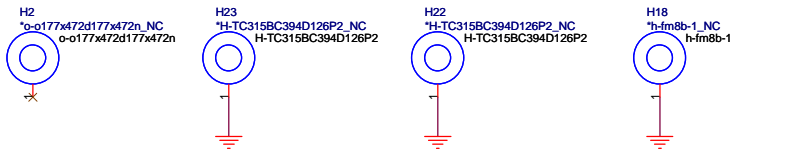
FOR CPU use



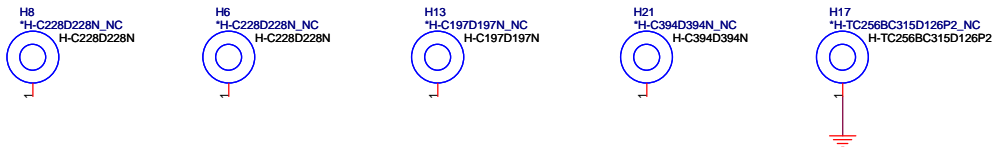
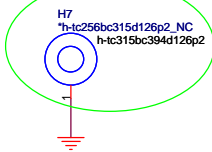
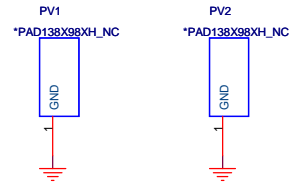
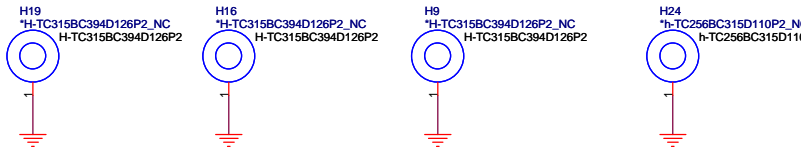
For MiniCard nut use.
on 31' header




For GPU nut use.

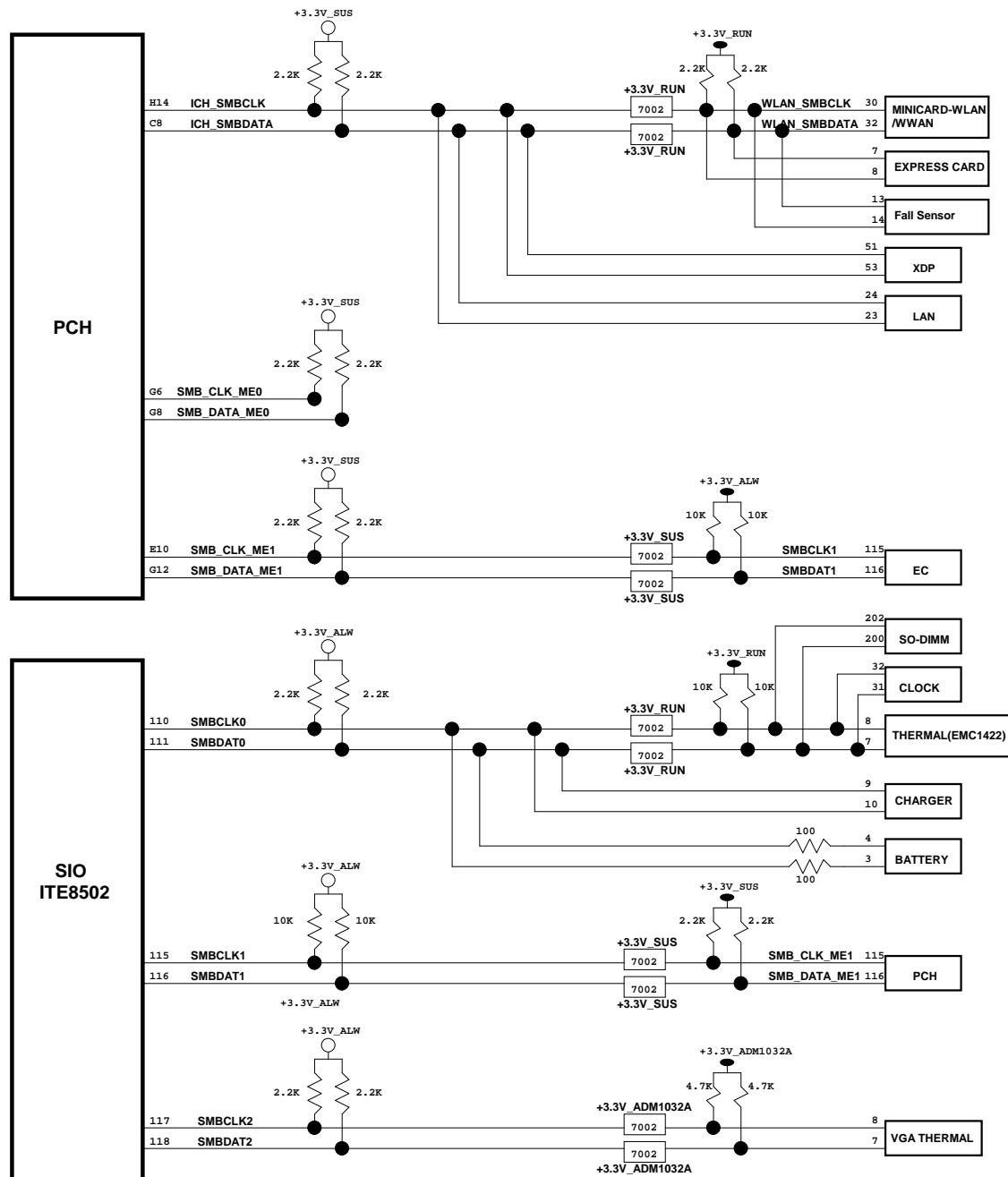


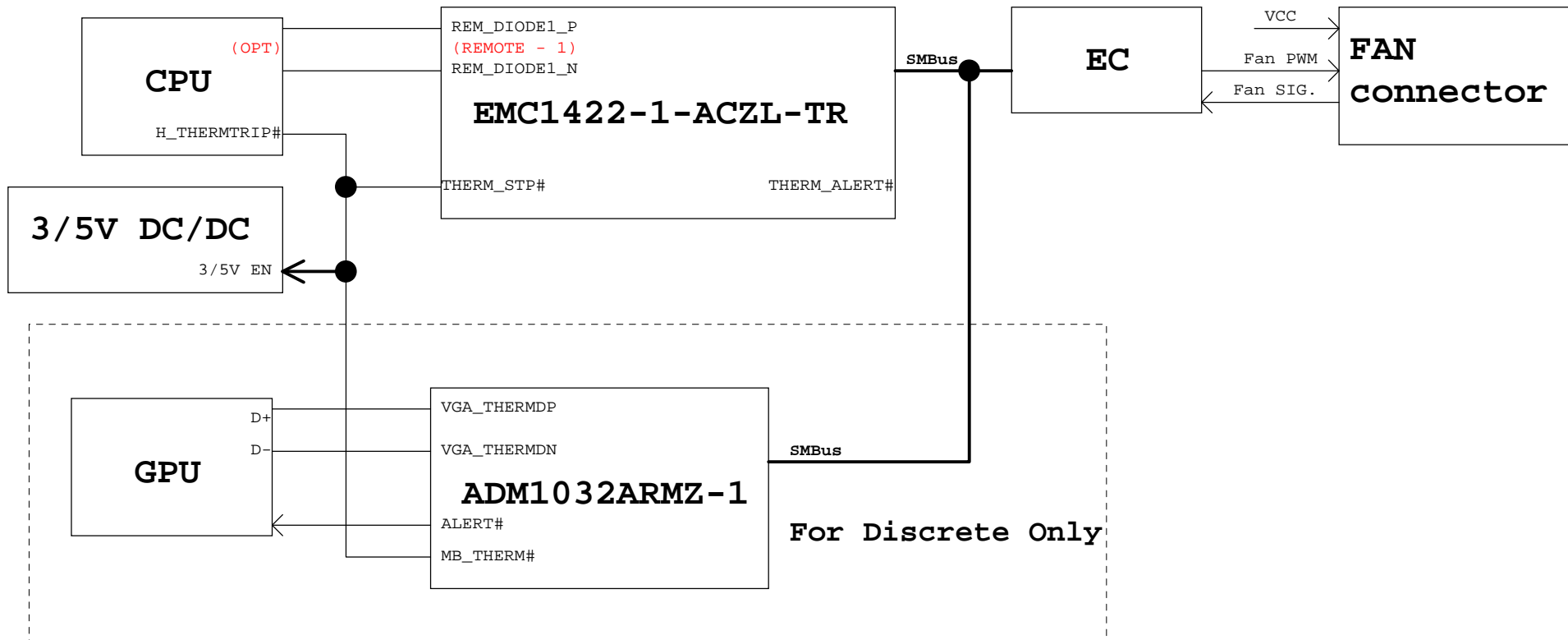
For PCH nut use.

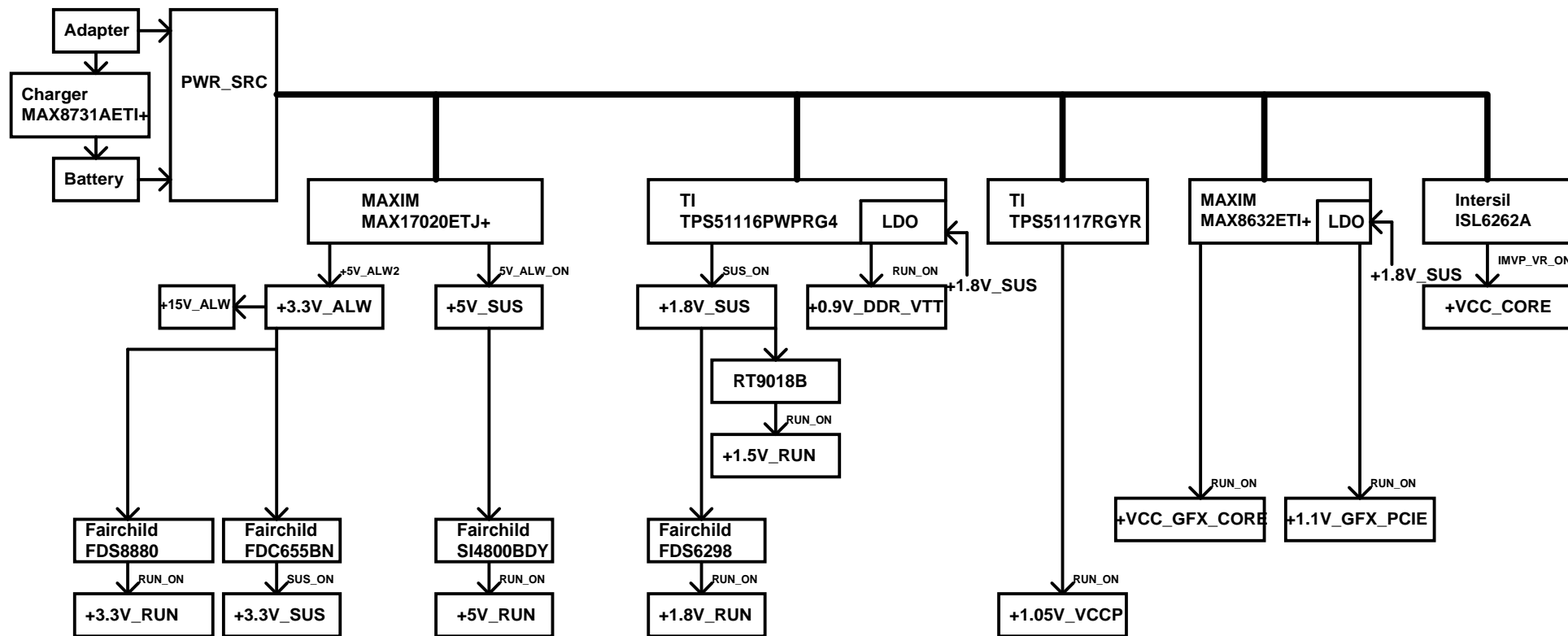


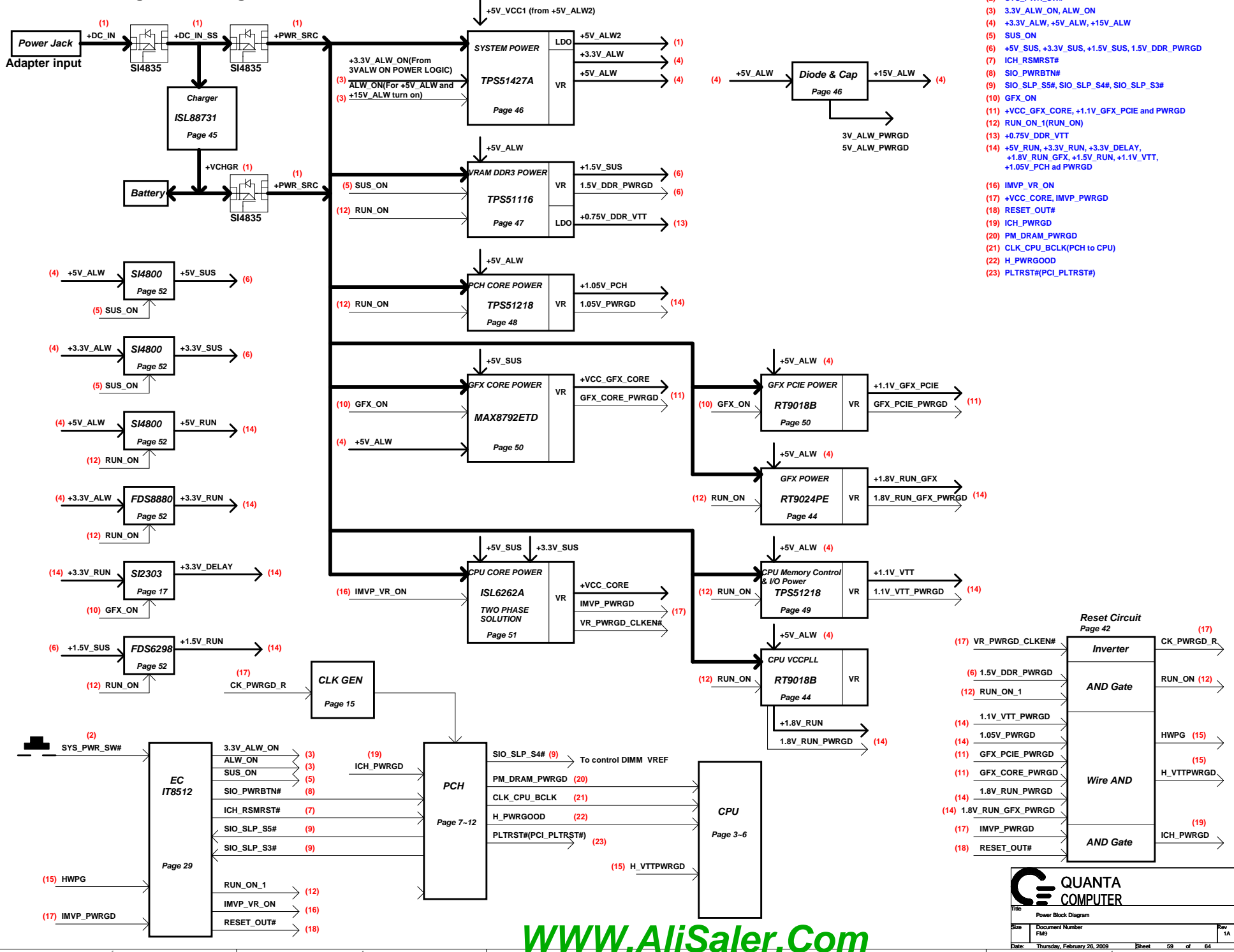
Title SCREW PAD		
Size FM9	Document Number FM9	Rev 1A
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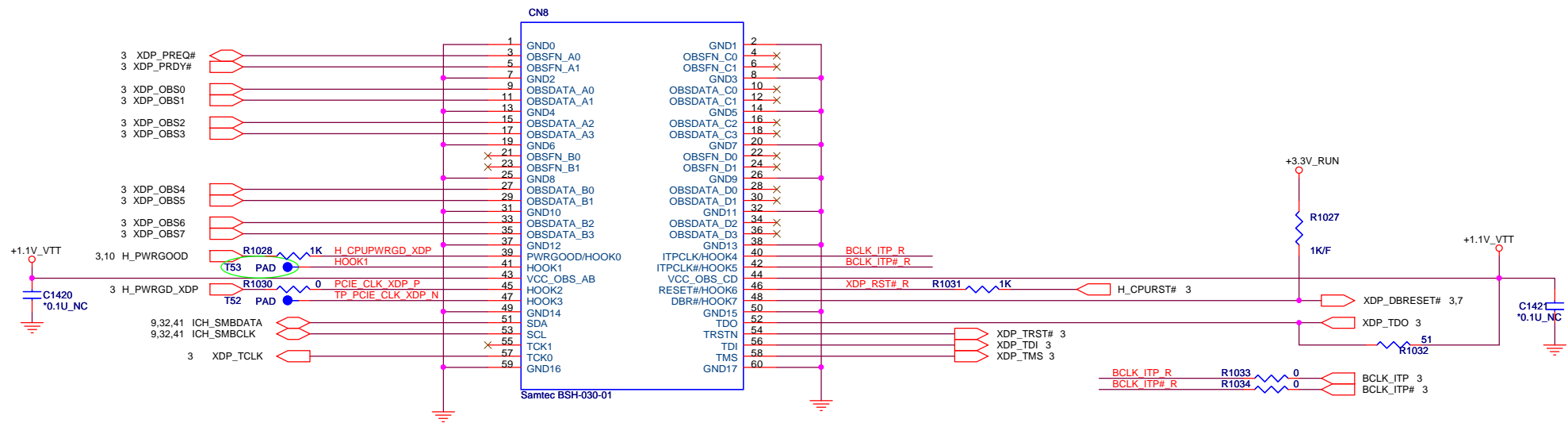
 QUANTA COMPUTER		
Title EMI CAP		
Size FM9	Document Number	Rev 1A
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 QUANTA COMPUTER		Title SMBUS BLOCK
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